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# ELECTRONIC DESIGN

18 OCT 1994

JULY 11, 1994

FOR ENGINEERS AND ENGINEERING MANAGERS—WORLDWIDE

## SLIC CHIP ELIMINATES RELAYS FROM TELEPHONE-SYSTEM LINE CARDS

## GETTING A BETTER HANDLE ON DSP:

- FOR IF SYSTEM DESIGN
- TO EXPLOIT UNDERSAMPLING
- BLAZING-FAST ADC POWERS ALL-DIGITAL CELLULAR BASE STATION
- COMPUTERS/ EMBEDDED SYSTEMS DESIGN SECTION
- PEASE PORRIDGE

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QUICKLOOK

VH-Design; Volker Hübel, München,

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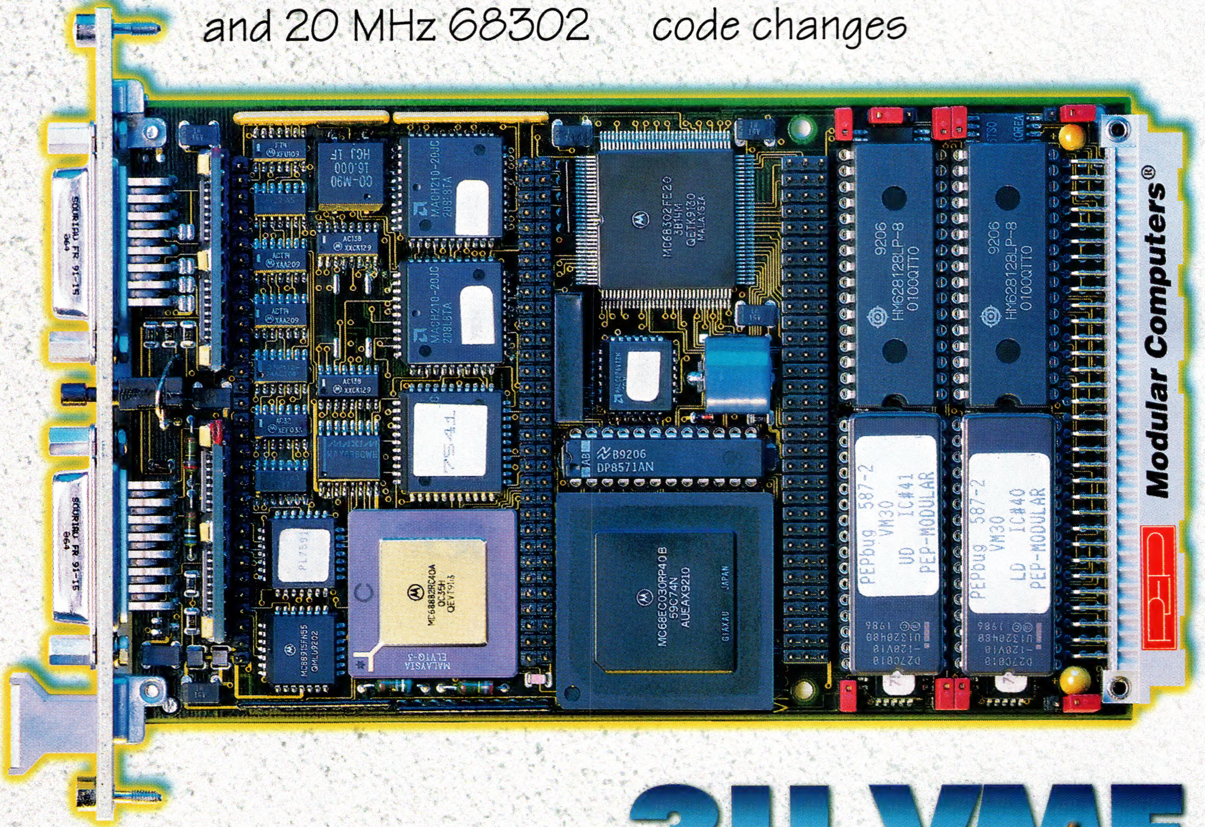

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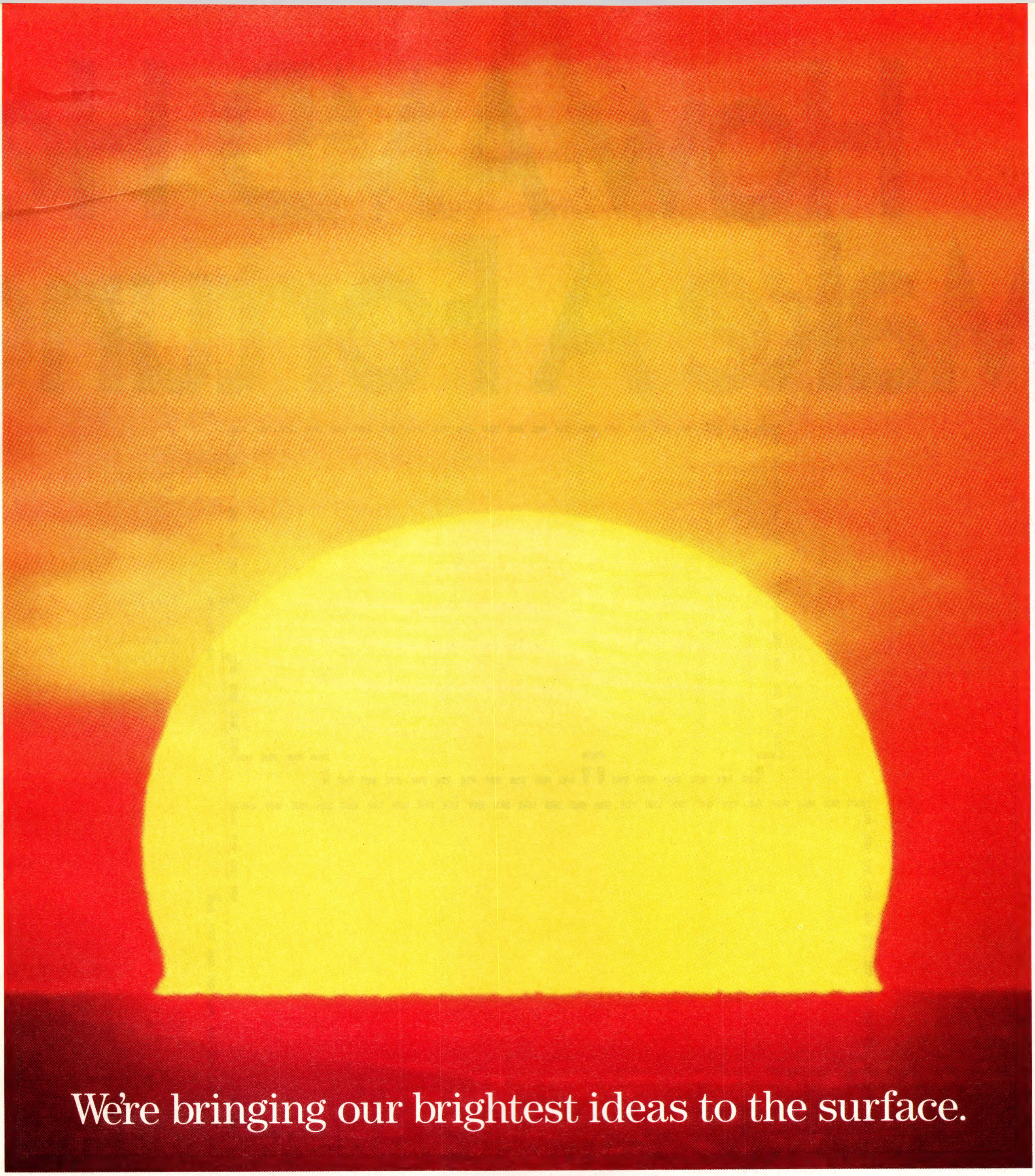

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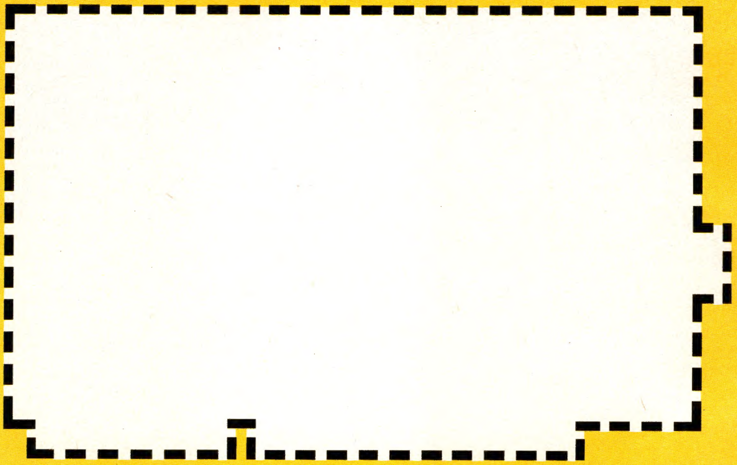

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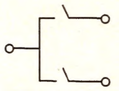

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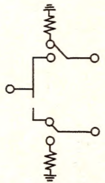

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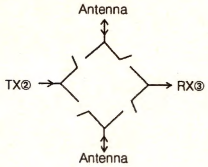

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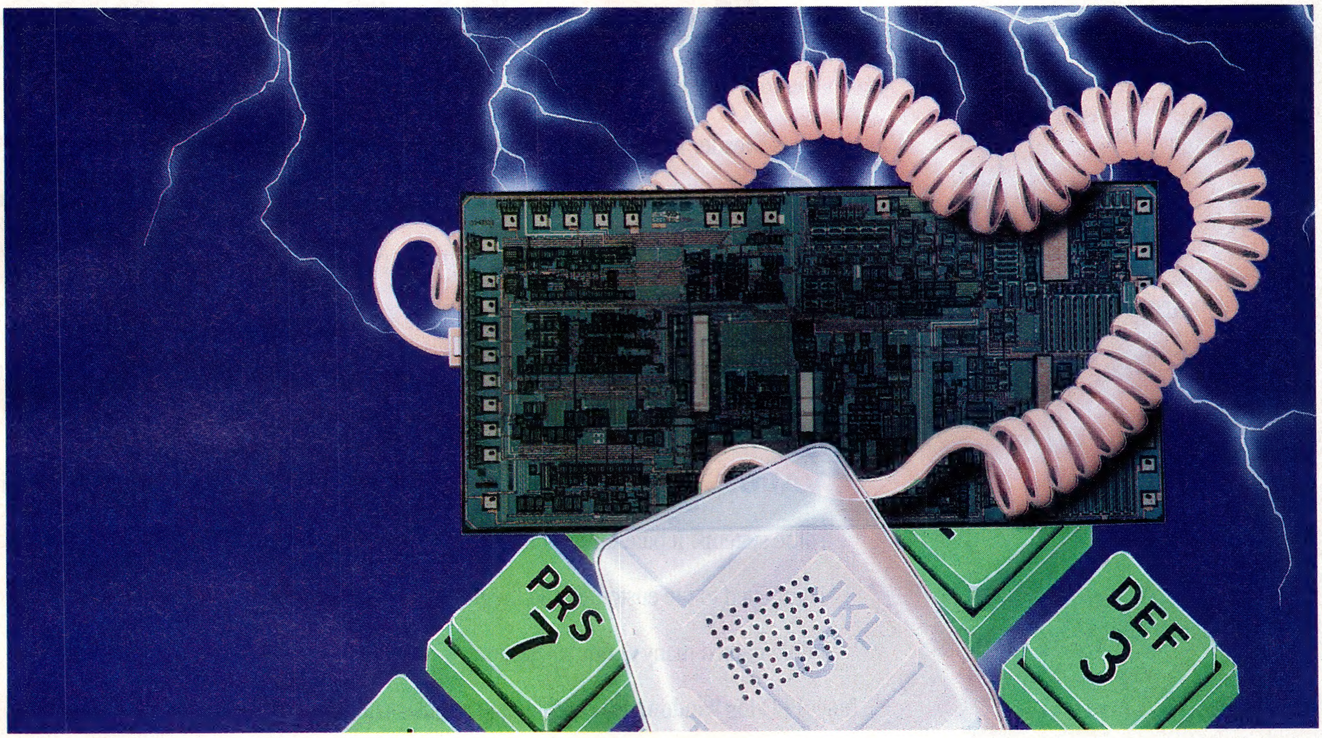

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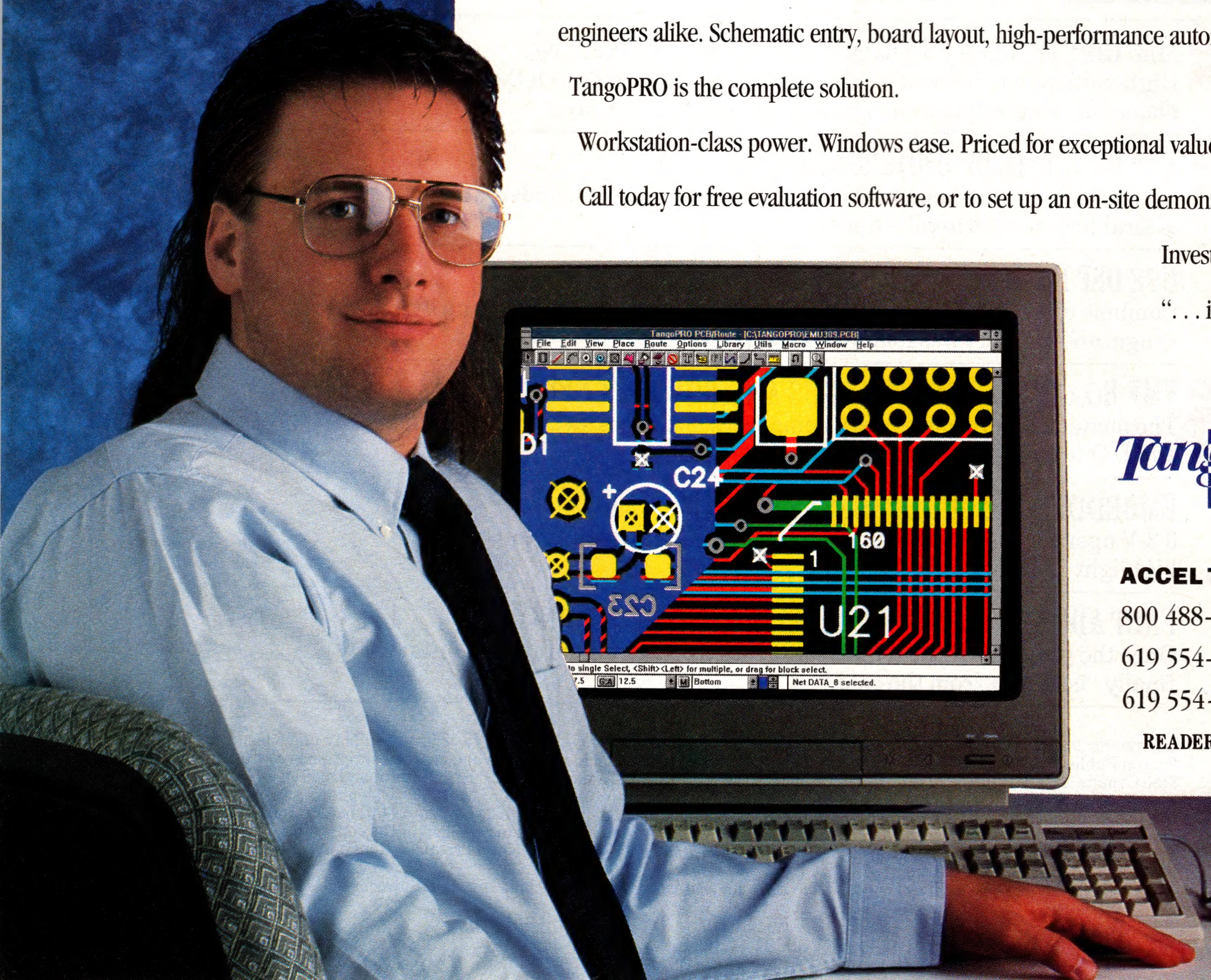
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Ideas for Design
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Jesse H. Neal Editorial
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1967 First Place Award
1968 First Place Award
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1975 Two Certificates of Merit
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1978 Certificate of Merit
1980 Certificate of Merit
1986 First Place Award
1989 Certificate of Merit
1992 Certificate of Merit

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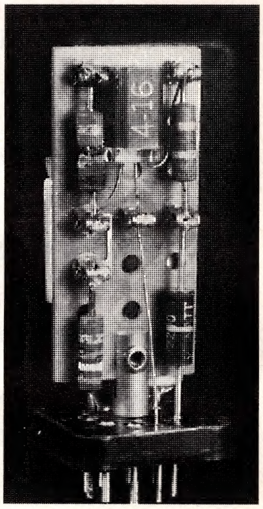
# ELECTRONIC DESIGN 40 YEARS AGO

### Plug-in transistor circuits

Plug-in transistor circuits, known as "Lee-Pacs", that offer savings in both the development and manufacture of transistorized equipment are available in five basic circuit types. All mounted on a standard 9-pin base in the same size can, the units include an audio amplifier, a cathode follower, two pulse generators, and a sine-wave oscillator. The units all weight about 1 oz.



The audio amplifier has an input impedance of 60 ohms and an output impedance of 10,000 ohms. Power out at 1kc with an input of 0.04v peak-to-peak is 1/2mw. Direct current bias power is 36mw. There is less than 1/2db change in output with ±15% change in bias. The cathode follower has an input impedance of 9000 ohms for a load of 1000 ohms. Power output with 4v peak-to-peak input signal (the maximum) is 2mw. Frequency response is flat from 20cy to nearly 10kc.

Both pulse generators require 27mw d-c power input with a load resistance of 270 ohms. The first type has a pulse frequency range of 10,000 to 50,000 pulses per sec for a pulse width of about 1μsec. The second has a pulse frequency range of 500 to 10,000 pulses per sec for a pulse width of about 6μsec. Frequency for both types varies less than –4% for a –20% change in bias voltage. Any frequency between 50cy and 100kc can be specified for the sine-wave oscillator. Power output is 2.25mw for a d-c power input of 200mw. Dimensions of the units are 2-3/16" x 29/32" x 29/32". They are manufactured by Lee Laboratories, Genesee, Pa., who plans to introduce other circuits of this size.*(Electronic Design, July 1954, p. 22.)*

*Already, companies were taking advantage of the transistor's size advantages, producing modular, complete-function circuits.—SS*

### Parachute test system

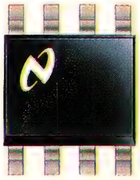
By means of an f-m transmitter mounted inside a dummy, strain-test data produced when the dummy is dropped by experimental parachutes is transmitted to recording instruments on the ground in a system developed to test new parachutes demanded by faster aircraft and airborne tactics. The system was devised by M.L. Greenough, C.C. Gordon, and associates of the National Bureau of Standards, Washington, D.C., for the Navy Bureau of Aeronautics.

The strain gages are arranged to read tension in the various harness straps. Seven measurement channels and a calibration channel are provided. At the ground station, a spot on the face of a cathode-ray tube moves up and down with the amplitude of the modulating signal. This spot is recorded on continuously moving photographic film.

Modulation of the transmitter with the signal from one channel at a time is accomplished by means of a "coder" of novel design. The coder supplies a series of time-sequential pulses to eight resistance bridges—one for the altimeter, one for each of six tensiometers, and one fixed bridge for calibration.

The bridge-unbalance signals are first amplified and then converted to amplitude modulation of a 15kc subcarrier. This subcarrier in turn frequency-modulates the 217Mc transmitter by means of a reactance-tube modulator. The ground-station receiver gives an output that is identical with the a-m 15kc subcarrier in the airborne unit. Demodulator and filter circuits convert this output signal to a waveform identical to the original bridge-unbalance signals. The transmitter's output is about 0.75w; range is 2 to 10 miles. Seven tubes are required. The battery pack, which provides 7.2v at 1 amp and 190v at 80ma, is tailored for about 1 hour of service.*(Electronic Design, July 1954, p. 10.)*

*Vacuum tubes were the workhorses through much of the 1950s. Although this module's seven tubes drained the batteries in about 1 hour, the unit apparently did its job (how many parachute descents last a full hour?).—SS*



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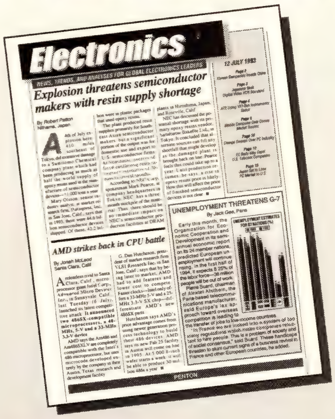

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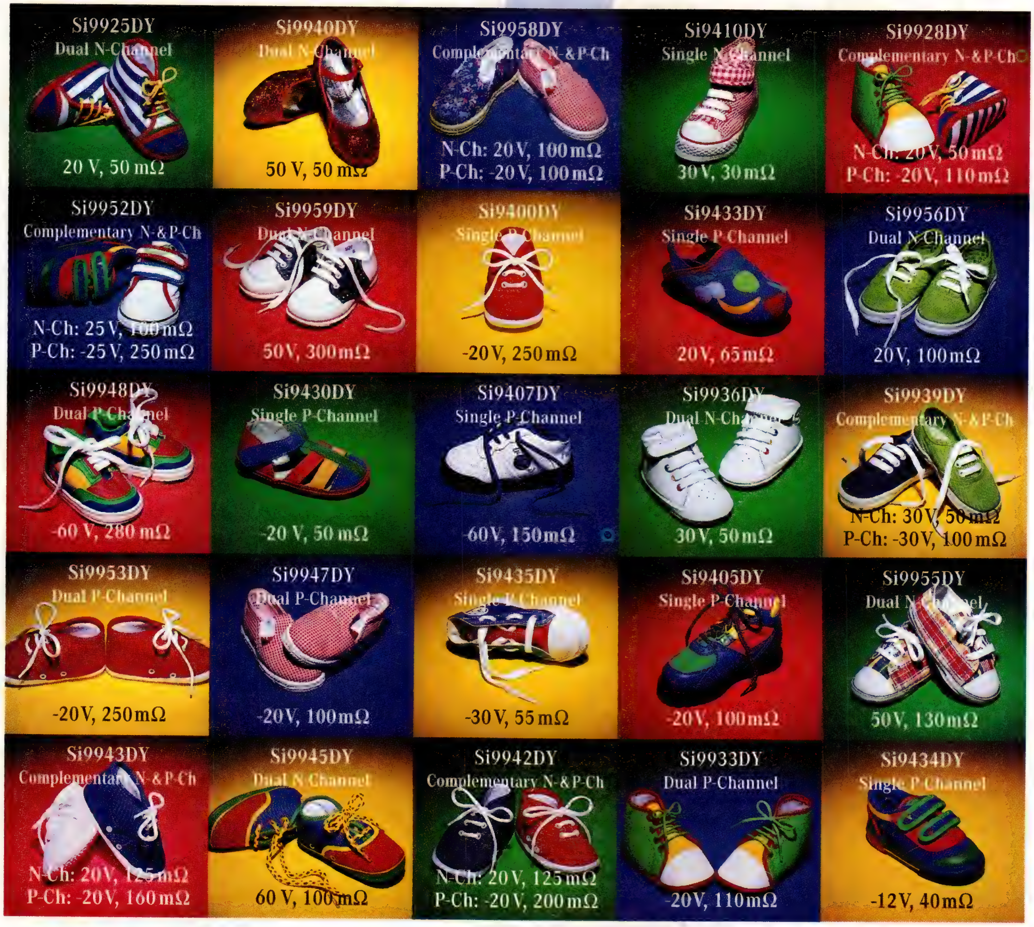

| | | | | |
|---|---|---|---|---|
| Si9925DY<br>Dual N-Channel<br>20 V, 50 mΩ | Si9940DY<br>Dual N-Channel<br>50 V, 50 mΩ | Si9958DY<br>Complementary N-&P-Ch<br>N-Ch: 20V, 100mΩ<br>P-Ch: -20V, 100mΩ | Si9410DY<br>Single N-Channel<br>30V, 30mΩ | Si9928DY<br>Complementary N-&P-Ch<br>N-Ch: 20V, 50mΩ<br>P-Ch: -20V, 110mΩ |
| Si9952DY<br>Complementary N-&P-Ch<br>N-Ch: 25V, 100mΩ<br>P-Ch: -25V, 250mΩ | Si9959DY<br>Dual N-Channel<br>50V, 300mΩ | Si9400DY<br>Single P-Channel<br>-20V, 250mΩ | Si9433DY<br>Single P-Channel<br>20V, 65mΩ | Si9956DY<br>Dual N-Channel<br>20V, 100mΩ |
| Si9948DY<br>Dual P-Channel<br>-60 V, 280 mΩ | Si9430DY<br>Single P-Channel<br>-20 V, 50 mΩ | Si9407DY<br>Single P-Channel<br>-60V, 150mΩ | Si9936DY<br>Dual N-Channel<br>30V, 50mΩ | Si9939DY<br>Complementary N-&P-Ch<br>N-Ch: 30V, 50mΩ<br>P-Ch: -30V, 100mΩ |
| Si9953DY<br>Dual P-Channel<br>-20V, 250mΩ | Si9947DY<br>Dual P-Channel<br>-20V, 100mΩ | Si9435DY<br>Single P-Channel<br>-30V, 55mΩ | Si9405DY<br>Single P-Channel<br>-20V, 100mΩ | Si9955DY<br>Dual N-Channel<br>50V, 130mΩ |
| Si9943DY<br>Complementary N-&P-Ch<br>N-Ch: 20V, 125mΩ<br>P-Ch: -20V, 160mΩ | Si9945DY<br>Dual N-Channel<br>60 V, 100mΩ | Si9942DY<br>Complementary N-&P-Ch<br>N-Ch: 20V, 125mΩ<br>P-Ch: -20V, 200mΩ | Si9933DY<br>Dual P-Channel<br>-20V, 110mΩ | Si9434DY<br>Single P-Channel<br>-12V, 40mΩ |

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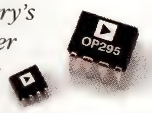
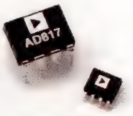


*The dual OP295 is the industry's highest accuracy,lowest power true rail-to-rail amplifier for single-supply applications.*



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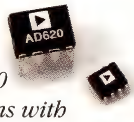

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# Design delays taking their

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| | Altera FLEX | Typical Gate Array |
|---|---|---|
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| Up Front NRE Cost | No | Yes |
| Production Lead Time | Off the Shelf | 8 – 12 Weeks |
| Reprogrammability | Yes | No |
| In-Circuit Reconfigurability | Yes | No |
| Flexibility for Design Changes | High | Low |
| Industry Standard CAE Support (VHDL, Verilog) | Yes | Yes |

Programmable logic rolls into new territory with the introduction of Altera's latest FLEX 8000 device, the 16,000 gate EPF81500. Now you can speed past unnecessary delays on the way to shipping your end product.

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# EDITORIAL

## INFORMATION SUPERHYPEWAY

I seem to have struck a resonant chord in my editorial on the Information Superhighway a few issues ago. Several readers have already expressed strong opinions about the hype that has unfortunately come to define the concept in many minds. In fact, one engineer in San Jose recently suggested that it should really be called the SuperHypeway.

There is also news from North Carolina, where I'm told there's an aggressive pilot program for connecting schools, universities, and some corporations. Although the idea isn't necessarily a bad one, an engineer who works in Research Triangle Park tells me that the governor and the legislators of the Tar Heel state are going bonkers over it.

I tend to agree with Buckminster Fuller's two-word definition of politics as "active ignorance" (I also tend to think that Bucky was referring to the process of politics as opposed to taking a broad swipe at all politicians). The definition also seems to work in North Carolina, which is likely to find itself leading the way in discovering the downside of e-mail ubiquity.

In its typical mad rush to overexpose anything new, a television news team in North Carolina found a marketing type who gleefully concluded that he could e-mail his company's advertisement to 30 million Internet addresses for just a few dollars in connection charges.

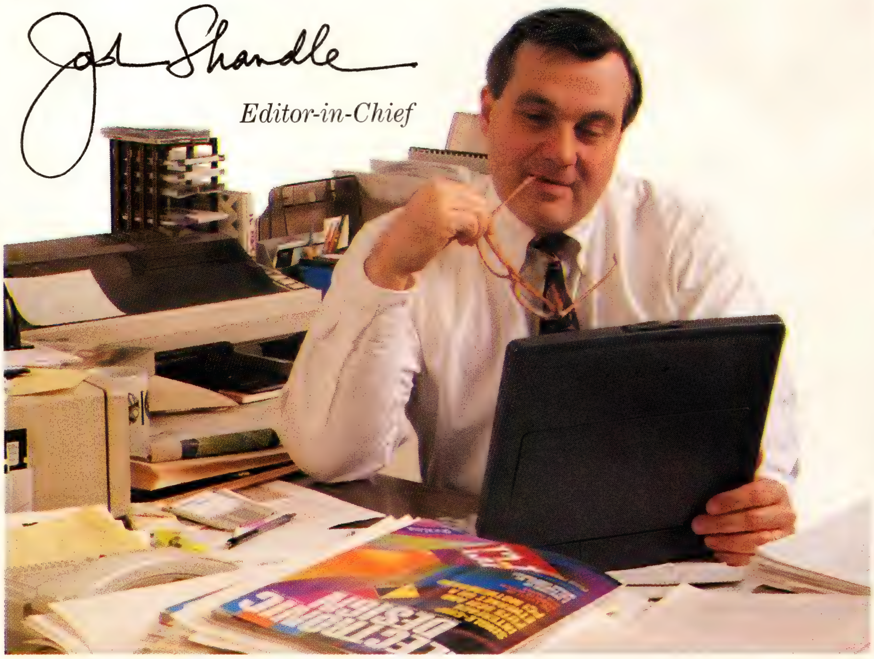
There are two problems with this scenario. First, the TV folks are lumping the Internet with the Information Superhighway, which is still mostly a figment of the imagination. In other words it is many things to many people. Second, the marketing maven doesn't understand that the Internet isn't for advertising. Hopefully, Mr. Marketer will receive 30 million pieces of flame mail in his in-box the morning after his advertising blitzkrieg.

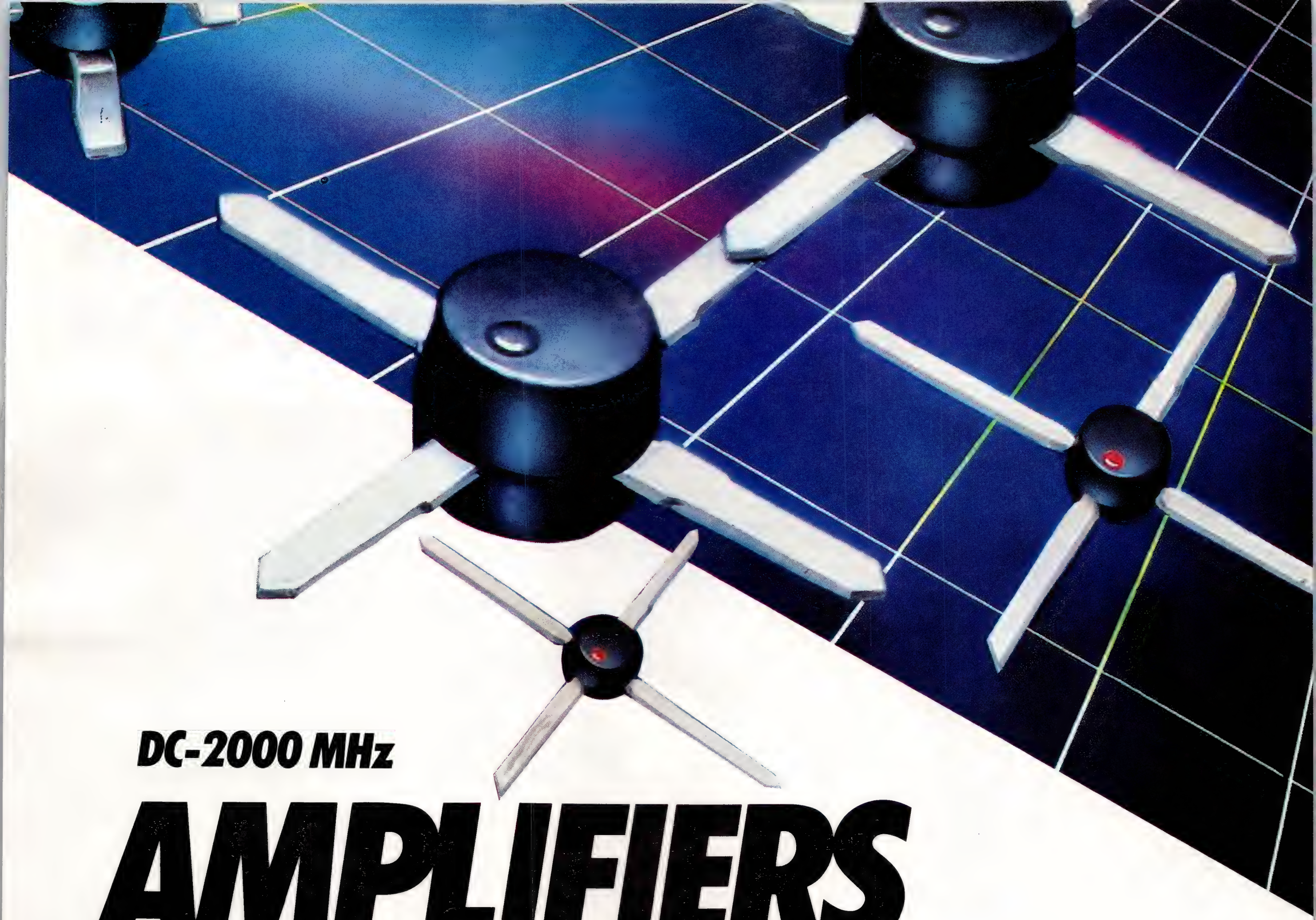
As someone who is relatively new to the Internet (I got my address about a year ago), I can already see its value and the potential for misuse. One thing I can do about it is to try to address the ignorance part of Bucky Fuller's definition. Ignorance is the enemy, and *Electronic Design* will most certainly raise its voice in opposition to anything that will threaten the value of the Internet.

If our readers have anything to pass on to the folks in Washington, or, California, or North Carolina, or anywhere this column is read, please let us know at edesign@class.org.

Josh Shandle

*Editor-in-Chief*





## DC-2000 MHz

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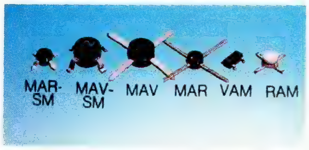

Models above shown actual size

*from* **99¢** Unit price $ (25 qty)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| PLASTIC SURFACE-MOUNT | | | ++VAM-3<br>1.45 | | +VAM-6<br>1.29 | ++VAM-7<br>1.75 | | |
| add suffix SM to model no. (ex. MAR-ISM) | MAR-1<br>1.04 | MAR-2<br>1.40 | MAR-3<br>1.50 | MAR-4<br>1.60 | MAR-6<br>1.34 | MAR-7<br>1.80 | MAR-8<br>1.75 | |
| | MAV-1<br>1.15 | +MAV-2<br>1.45 | +MAV-3<br>1.55 | MAV-4<br>1.65 | | | | MAV-11<br>2.15 |
| CERAMIC SURFACE-MOUNT | RAM-1<br>4.95 | RAM-2<br>4.95 | RAM-3<br>4.95 | RAM-4<br>4.95 | RAM-6<br>4.95 | RAM-7<br>4.95 | RAM-8<br>4.95 | |
| PLASTIC FLAT-PACK | MAV-1<br>1.10 | +MAV-2<br>1.40 | +MAV-3<br>1.50 | +MAV-4<br>1.60 | | | | MAV-11<br>2.10 |
| | MAR-1<br>0.99 | MAR-2<br>1.35 | MAR-3<br>1.45 | MAR-4<br>1.55 | MAR-6<br>1.29 | MAR-7<br>1.75 | MAR-8<br>1.70 | |
| Freq.MHz,DC to | 1000 | 2000 | 2000 | 1000 | 2000 | 2000 | 1000 | 1000 |
| Gain, dB at 100MHz | 18.5 | 12.5 | 12.5 | 8.3 | 20 | 13.5 | 32.5 | 12.7 |
| Output Pwr. +dBm | 1.5 | 4.5 | 10.0 | 12.5 | 2.0 | 5.5 | 12.5 | 17.5 |
| NF, dB | 5.5 | 6.5 | 6.0 | 6.5 | 3.0 | 5.0 | 3.3 | 3.6 |

Notes: + Frequency range DC-1500MHz    ++ Gain 1/2 dB less than shown

designer's amplifier kits
***DAK-2:*** 5 of each MAR-model (35 pcs), only $59.95
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designer's chip capacitor kit
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chip coupling capacitors at .12¢ each (50 min.)

| Size (mils) | Value |
|---|---|
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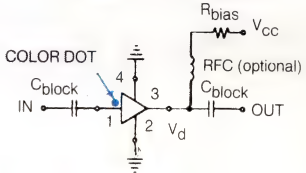
| 80 x 50 | 1000, 2200, 4700, 6800, 10,000 pf |
| 120 x 60 | .022, .047, .068, .1 µf |

Typical Circuit Arrangement



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| | KM44S4020AT-12 | 83MHz | 4096cycle/64ms |
| | KM44S4020AT-13 | 77MHz | 4096cycle/64ms |
| 2M×8 | KM48S2020AT-10 | 100MHz | 4096cycle/64ms |
| | KM48S2020AT-12 | 83MHz | 4096cycle/64ms |
| | KM48S2020AT-13 | 77MHz | 4096cycle/64ms |

* All Products meet JEDEC Standard

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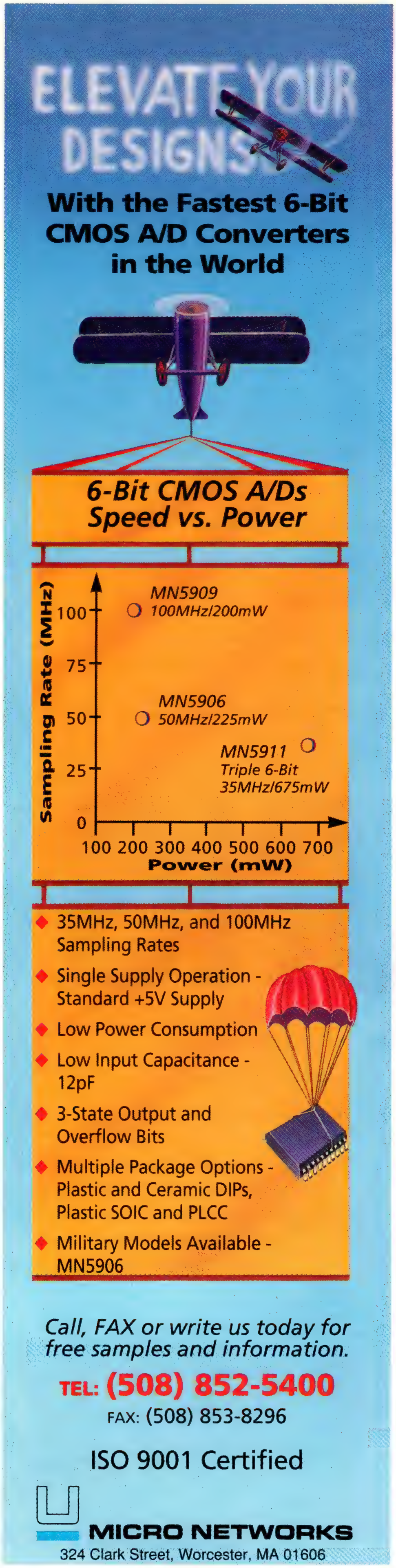
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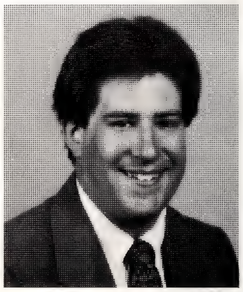
# PCI: HERE, THERE, EVERYWHERE

Traditionally, when PC designers look for ways to increase the performance of peripherals such as disk drives and graphics accelerators, they'll resort to using a local bus. The first wave of these buses consisted of proprietary alternatives that weren't compatible with each other. That was followed by the VL-Bus, which gained a reputation as an inexpensive "quick fix." Though VL-Bus systems are currently shipping in very large volumes, designers now are turning to the PCI bus, which has taken the computing industry by storm.

The PCI bus, originally developed by Intel, isn't just a desktop local bus anymore. PCI is becoming the local bus of choice for systems ranging from portables to those built with high-performance VMEbus and Futurebus+ boards, and in applications ranging from multimedia and accelerated graphics to multiprocessing. The PCI Special Interest Group (SIG) claims that 10 million PCs will ship with a PCI bus in 1994 and 30 million in 1995, roughly 75% of all systems.


RICHARD NASS
COMPUTER SYSTEMS

The PCI SIG, which is the organization that controls the specification, revealed it will release a design guide by the end of the summer that enables developers of most types of portable equipment to integrate the PCI bus within their designs. This includes products ranging from systems to components and PCMCIA peripherals.

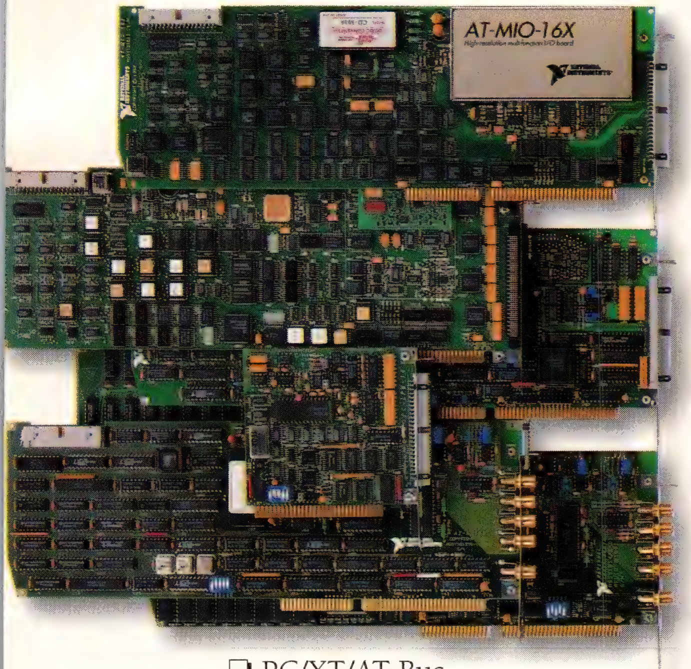
The guide offers tips and rules on how to connect 32-bit components, which are typically found in desktop PCs, to the PCI bus. Among the components discussed are graphics accelerators, hard-disk drives, and network adapters. The guide also shows designers how to implement a power-savings feature, the clock run-down pin, that lets users power-down the system clock. In addition, because the industry's eventual move from 5-V logic to 3.3 V will carry over to the PCI bus, techniques for implementing the lower voltage are described.

Another move to put the PCI bus into portable systems comes from the development of the Cardbus. The PCI SIG and the PCMCIA technical committee are jointly developing the Cardbus standard, which should be included in the next release of the PCMCIA specification. The 32-bit bus basically forms a bridge between the PCMCIA and PCI buses. Components that may possibly connect to the Cardbus include disk drives and network adapters. This means that those PCMCIA-based components would reach the same performance level as their add-in-card counterparts, which is higher than what's currently achieved by the PCMCIA bus.

PCI also is making its presence felt in high-end systems. The VMEbus and Futurebus+ markets have put their own spin on PCI and created the PMC (PCI Mezzanine Card). The PMC connects through a mezzanine interface, as if there weren't already enough mezzanine specifications for VMEbus boards. It's a subset of the PCI specification that offers a lower physical profile than the standard PCI modules found in PCs. In the PMC standard, the PCI bus acts as a local connection between the processor-memory array and the system peripheral controllers, just as is the case with the PC. The PMC is defined under IEEE specification P1386.1. The scope of the specification is to define a family of cards for VMEbus, Futurebus+, and other high-end systems. The PMC specification uses electrical and logical layers that are similar to PCI, yet physically different.

A VMEbus board that contains a PMC module still fits the VME form factor in one slot. The PMC's high bandwidth can transfer 132 Mbytes/s in 32-bit mode and 264 Mbytes/s using 64 bits—the same as a PCI peripheral. On typical VMEbus boards, the module can connect either through the baseboard's front panel or its P2 connector. The first PMC modules will include graphics, FDDI, ATM, and other high-performance I/O.

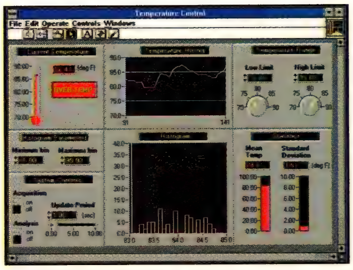
# Multiple Choice.



☐ PC/XT/AT Bus

☐ Parallel Port

☐ PCMCIA



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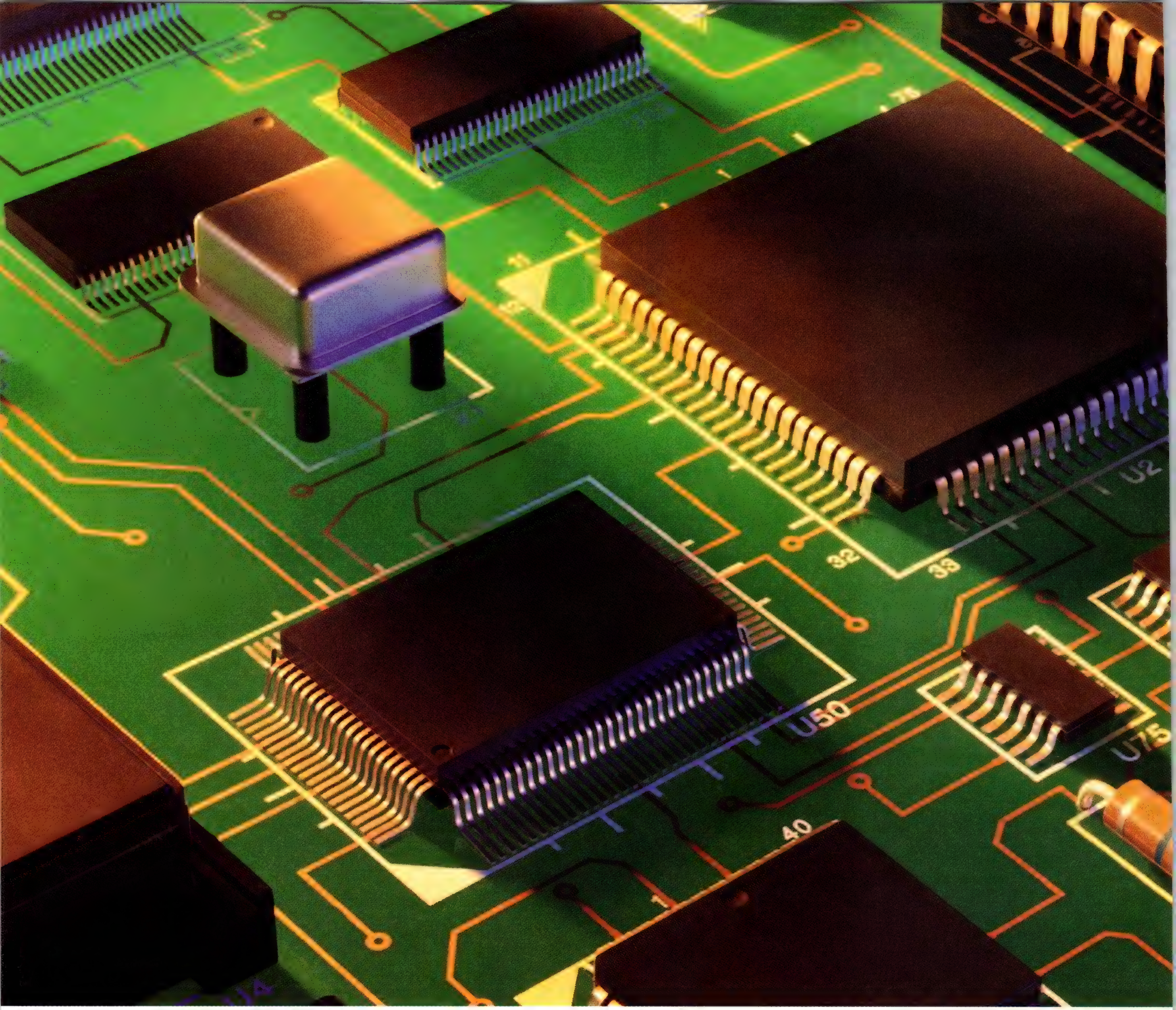

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| DEVICE | MACROCELLS | $t_{PD}$ | I/O | $I_{CC}$ |
|---|---|---|---|---|
| iFX8160 | 160 | 10ns | 168 | 2.5mA/MHz |
| iFX780 | 80 | 10ns | 102 | 1.5mA/MHz |
| iFX760 | 60 | 10ns | 60 | 1.5mA/MHz |
| iFX740 | 40 | 10ns | 50 | 1mA/MHz |
| iFX730 | 30 | 10ns | 30 | 1mA/MHz |

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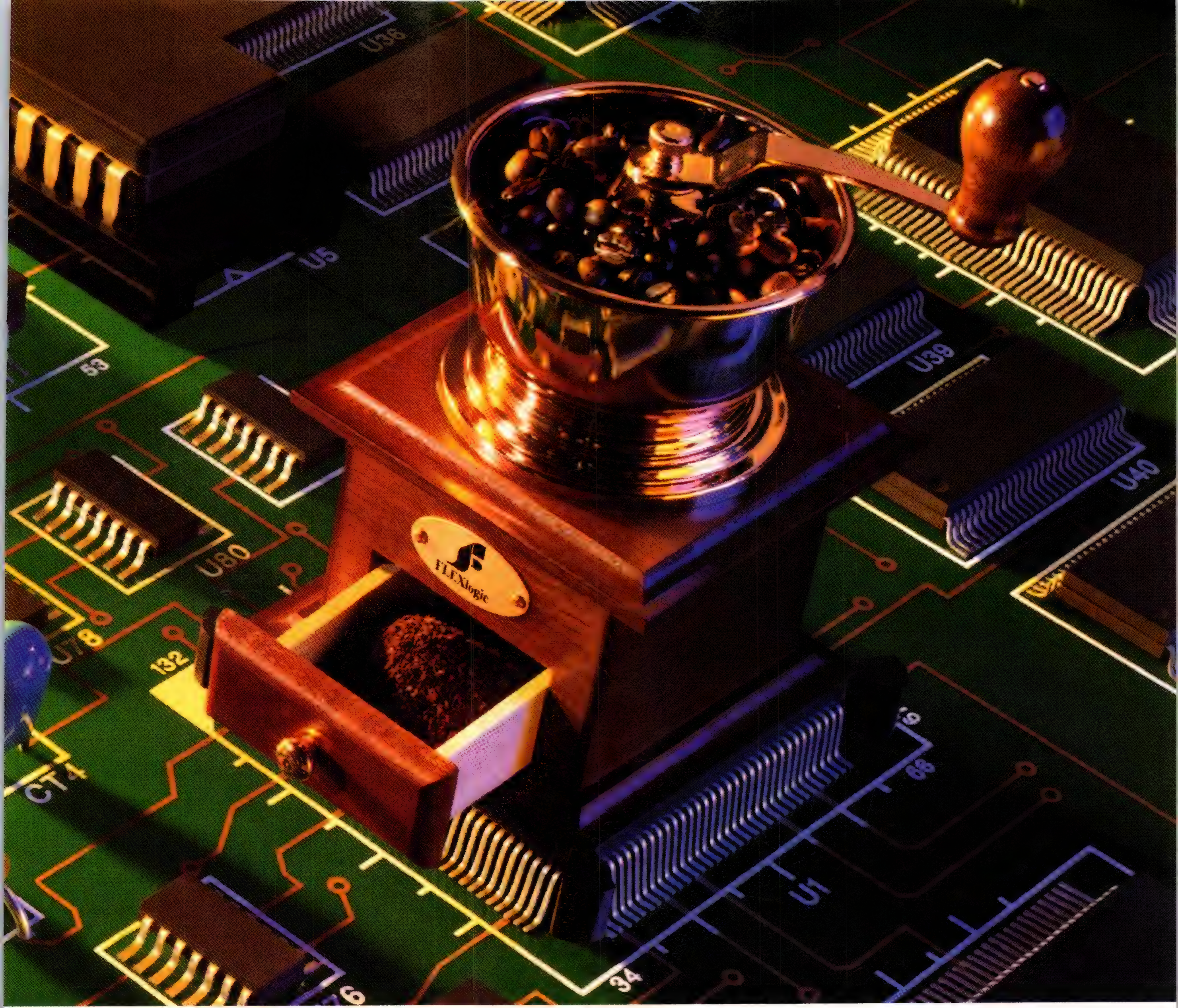

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# UPCOMING MEETINGS

## JULY

**2nd IEEE Workshop on Real-Time Applications, July 21-22.** Washington D.C. Contact Alexander D. Stoyenko, Real-Time Computing Lab, Computer & Information Science, New Jersey Institute of Technology, University Heights, Newark, NJ 07102; (201) 596-5765; fax (201) 596-5777; E-mail: Alex@vulcan.njit.edu.

**IEEE Power Engineering Society Summer Meeting, July 24-28.** Hilton Hotel, San Francisco, CA. Contact Eva Tiffer, Pacific Gas & Electric Co., Mail Code B23C, P.O. Box 770000, San Francisco, CA 94105; (415) 973-2875; fax (415) 972-6011.

## AUGUST

**MACWORLD Expo/Boston, Aug. 2-5.** Bayside Expo & World Trade Center, Boston, MA. Contact Mitch Hall & Associates at (617) 361-2001.

**3rd IEEE International Symposium on High Performance Distributed Computing, Aug. 3-5.** Westin St. Francis Hotel, San Francisco, CA. Contact Geoffrey C. Fox, NPAC Director, Room 3-228, 111 College Pl., Syracuse, NY 13244-4100; (315) 443-4741; fax (315) 443-1973; E-mail: Gcf@pac.syr.edu.

**4th IEEE Workshop on Computers in Power Electronics, Aug. 7-10.** The Universite du Quebec, Trois-Rivieres, Quebec, Canada. Contact Adam Skorek, Dept. d'Ingenierie, UQTR, C.P. 500, Trois-Rivieres, Quebec G9A 5H7, Canada; (818) 376-5071 ext. 3929; fax (819) 376-5152.

**IEEE International Symposium on Applications of Ferroelectrics, Aug. 7-10.** Conference Center, University Park, PA. Contact Amar Bhalla, 253 MRL, Pennsylvania State University, University Park, PA 16802; (814) 865-9232.

**IEEE International Geoscience & Remote Sensing Symposium (IGARSS '94), Aug. 8-12.** California Institute of Technology, Pasadena, CA. Contact Tammy I. Stein, IEEE/GRSS, 2610 Lakeway Dr., Seabrock, TX 77586; (713) 291-9222; fax (713) 291-9224.

**IEEE Magnetic Recording Conference (IMRC '94), Aug. 16-20.** University of California, La Jolla, CA. Contact Roger F. Hoyt, IBM Almaden Research Center, 650 Harry Rd., K01/803, San Jose, CA 95120-6099; (408) 927-2118; fax (408) 927-3204.

**IEEE International Symposium on Electromagnetic Compatibility, Aug. 22-26.** Palmer House Hotel, Chicago, IL. Contact H.R. Hofmann, 1210 Lawn Meadow Ln., Naperville, IL 60540; (708) 979-3627; fax (708) 979-5755.

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# TECHNOLOGY NEWSLETTER

## 1.6-Gbit/s Spanceivers Hit The Market

Until now, AutoBahn—a technology that can move data at a theoretical rate of 1.6 Gbits/s—was just a concept on paper. With the announcement of the Spanceiver ICs, the concept has transformed into a reality. The chip, which was developed by Pep Modular Computers, Scottsdale, Ariz., is being fabricated in a 0.8-$\mu$m MOSAIC V positive ECL process at Motorola Semiconductor, Phoenix, Ariz. The AutoBahn Spanceiver IC, called the MC100SX1451, is a parallel-to-serial and serial-to-parallel transceiver that reduces latencies. The chip, housed in a 14-by-14-mm quad flat pack, should be available in the next few months. Sample prices range from $180 to $250, depending on quantity. To help developers get their AutoBahn products to market quickly, Pep is releasing a starter kit for VMEbus designs. The kit comes with two Spanceivers, each on a small mezzanine board that plugs into the VME backplane in a specially terminated slot. The mezzanine also comes with 128 kbytes of 20-ns static RAM, a fast GAL that contains the logic circuitry required to connect the parallel interface to a 32-bit data source, an address counter, and the serial interface to pins 21 and 22 on the P1 connector of the VMEbus backplane. The kit also includes a 68030-based CPU board and a backplane. It sells for $4990. For more information about the Spanceivers or the kit, call Pep at (602) 483-7100, or Motorola at (602) 655-5734. *RN*

## Fiber-Optic Sensor Boasts Low Cost

Under an effort funded by the U.S. Dept. of Energy, scientists at Lawrence Livermore Laboratory, Livermore, Calif., have developed a fiber-optic sensor to detect contaminants. Boasting a low-cost, portable design, the sensor was originally developed to sample ground contamination at the Savannah River Technology Center in Georgia. The sensor features a chemical reagent that turns intensely red when exposed to specific chlorinated compounds, such as trichloroethylene (TCE), with the intensity of the color being proportional to the contaminant concentration. Its high accuracy and ability to offer immediate results provide a viable option to current sampling and analysis methods. Lawrence Livermore Laboratory is in the process of transferring this technology to the private sector. Licensing agreements are already underway. They include deals with Purus Inc., San Jose, Calif., which will use the sensor as an industrial monitor, and with Burge Instruments, Tempe, Ariz., which will use the sensor as a portable contaminant-measurement package. For further information, contact Gordon Yano in the Public Affairs Office at (510) 423-3117. *CA*

## True UTQFP Package Stands 0.8-mm Tall

A fully molded ultra-thin quad flat pack (UTQFP) has been developed with a mounted height of only 0.8 mm. The package, tooled by Silicon Systems, Tustin, Calif., addresses problems inherent to some UTQFPs that have preceded it. Although those packages have mounted heights in the range of 0.45 to 0.60 mm, they are actually half-molded packages that expose the bottom of the package at the pc-board level. Exposed metal is a source of reliability concerns. Silicon Systems's UTQFP is protected from ingress of moisture. The initial 64-lead version is JEDEC-compliant and has the same footprint as the company's TQFP and VTQFP packages. For more information, call Silicon Systems at (714) 573-6200. *DM*

## Group To Form Home Video On Demand

A group of hardware and software developers are banding together to deliver a standards-based, end-to-end system that supplies interactive two-way video-on-demand for end users. The system will employ such standards as ATM for communications and MPEG for video-signal compression. The adherence to standards ensures compatibility between data-storage equipment, fiber networks, and intelligent set-top devices. The proposal calls for the system to include a video and information server from Digital Equipment Corp., Maynard, Mass.; a fiber switched-network system from BroadBand Technologies Inc., Research Triangle Park, N.C.; set-top boxes from Philips Consumer Electronics Co., Knoxville, Tenn., and Compression Labs Inc., San Jose, Calif.; and software from Microware Systems Corp., Des Moines, Iowa. The interactive system will send ATM cells all the way to the set-top box, rather than to the final active node in the system. Transporting MPEG information in ATM packets, the system will deliver up to 1500 channels of interactive programming. For further information about the system, call BroadBand Technologies at (919) 405-4816. *RN*

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# dc to 3GHz from $11⁴⁵

## lowpass, highpass, bandpass

- less than 1dB insertion loss
- greater than 40dB stopband rejection
- surface-mount
- BNC, Type N, SMA available
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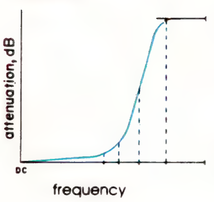
LOW PASS



### low pass, Plug-in, dc to 1200MHz

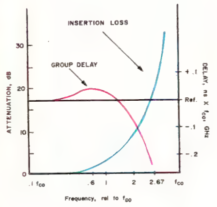
| Model No. | Passband MHz loss < 1dB | Stopband, MHz loss > 20dB | Stopband, MHz loss > 40dB | Model No. | Passband MHz loss < 1dB | Stopband, MHz loss > 20dB | Stopband, MHz loss > 40dB |
|---|---|---|---|---|---|---|---|
| ★LP-5 | DC-5 | 8-10 | 10-200 | ★LP-250 | DC-225 | 320-400 | 400-1200 |
| ★LP-10.7 | DC-11 | 19-24 | 24-200 | ★LP-300 | DC-270 | 410-550 | 550-1200 |
| ★LP-21.4 | DC-22 | 32-41 | 41-200 | ★LP-450 | DC-400 | 580-750 | 750-1800 |
| ★LP-30 | DC-32 | 47-61 | 61-200 | ★LP-550 | DC-520 | 750-920 | 920-2000 |
| ★LP-50 | DC-48 | 70-90 | 90-200 | ★LP-600 | DC-680 | 840-1120 | 1120-2000 |
| ★LP-70 | DC-60 | 90-117 | 117-300 | ★LP-750 | DC-700 | 1000-1300 | 1300-2000 |
| ★P-90 | DC-81 | 121-137 | 167-400 | ★LP-800 | DC-720 | 1080-1400 | 1400-2000 |
| ★LP-100 | DC-98 | 146-189 | 189-400 | ★LP-850 | DC-760 | 1100-1400 | 1400-2000 |
| ★LP-150 | DC-140 | 210-300 | 300-600 | ★LP-1000 | DC-900 | 1340-1750 | 1750-2000 |
| ★LP-200 | DC-190 | 290-390 | 390-800 | ★LP-1200 | DC-1000 | 1620-2100 | 2100-2500 |

Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

### Surface-mount, dc to 570MHz

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SCLF-21.4 | DC-22 | 32-41 | 41-200 | SCLF-190 | DC-190 | 290-390 | 390-800 |
| SCLF-30 | DC-30 | 47-61 | 61-200 | SCLF-380 | DC-380 | 580-750 | 750-1800 |
| SCLF-45 | DC-45 | 70-90 | 90-200 | SCLF-420 | DC-420 | 750-920 | 920-2000 |
| SCLF-135 | DC-135 | 210-300 | 300-600 | | | | |

Price, (1-9 qty), all models: $11.45

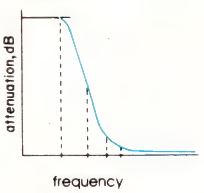


### Flat Time Delay, dc to 1870MHz

| Model No. | Passband MHz loss < 1.2dB | Stopband MHz loss > 10dB | Stopband MHz loss > 20dB | VSWR Freq. Range, DC thru 0.2fco X̄ | VSWR Freq. Range, DC thru 0.6fco X̄ | Group Delay Variations, ns Freq. Range, DC thru fco X̄ | Group Delay Variations, ns Freq. Range, DC thru 2fco X̄ | Group Delay Variations, ns Freq. Range, DC thru 2.67fco X̄ |
|---|---|---|---|---|---|---|---|---|
| ★BLP-39 | DC-23 | 78-117 | 117 | 1.3:1 | 2.3:1 | 0.7 | 4.0 | 5.0 |
| ★BLP-117 | DC-65 | 234-312 | 312 | 1.3:1 | 2.4:1 | 0.35 | 1.4 | 1.9 |
| ★BLP-156 | DC-94 | 312-416 | 416 | 0.3:1 | 1.1:1 | 0.3 | 1.1 | 1.5 |
| ★BLP-200 | DC-120 | 400-534 | 534 | 1.6:1 | 1.9:1 | 0.4 | 1.3 | 1.6 |
| ★BLP-300 | DC-180 | 600-801 | 801 | 1.25:1 | 2.2:1 | 0.2 | 0.6 | 0.8 |
| ★BLP-467 | DC-280 | 934-1246 | 1246 | 1.25:1 | 2.2:1 | 0.15 | 0.4 | 0.55 |
| ▲BLP-933 | DC-560 | 1866-2490 | 2490 | 1.3:1 | 2.2:1 | 0.09 | 0.2 | 0.28 |
| ▲BLP-1870 | DC-850 | 3740-6000 | 5000 | 1.45:1 | 2.9:1 | 0.05 | 0.1 | 0.15 |

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

HIGH PASS

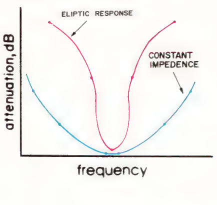


### high pass, Plug-in, 27.5 to 2200MHz

| Model No. | Stopband MHz loss < 40dB | Stopband MHz loss < 20dB | Passband, MHz loss < 1dB | VSWR Pass-band Typ. | Model No. | Stopband MHz loss < 40dB | Stopband MHz loss < 20dB | Passband, MHz loss < 1dB | VSWR Pass-band Typ. |
|---|---|---|---|---|---|---|---|---|---|
| ★HP-25 | DC-13 | 13-19 | 27.5-200 | 1.8:1 | ★HP-400 | DC-210 | 210-290 | 395-1600 | 1.7:1 |
| ★HP-50 | DC-20 | 20-26 | 41-200 | 1.5:1 | ★HP-500 | DC-280 | 280-365 | 500-1600 | 1.8:1 |
| ★HP-100 | DC-40 | 40-55 | 90-400 | 1.8:1 | ★HP-600 | DC-350 | 350-440 | 600-1600 | 2.0:1 |
| ★HP-150 | DC-70 | 70-95 | 133-600 | 1.8:1 | ★HP-700 | DC-400 | 400-520 | 700-1800 | 1.6:1 |
| ★HP-175 | DC-70 | 70-105 | 160-800 | 1.5:1 | ★HP-800 | DC-445 | 445-570 | 780-2000 | 2.1:1 |
| ★HP-200 | DC-90 | 90-116 | 185-800 | 1.6:1 | ★HP-900 | DC-520 | 520-660 | 910-2100 | 1.8:1 |
| ★HP-250 | DC-100 | 100-150 | 225-1200 | 1.3:1 | ★HP-1000 | DC-550 | 550-720 | 1000-2200 | 1.9:1 |
| ★HP-300 | DC-145 | 145-170 | 290-1200 | 1.7:1 | | | | | |

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

BANDPASS



### bandpass, Elliptic Response, 10.7 to 70MHz

| Model No. | Center Freq. (MHz) | Passband I.L. 1.5 dB Max. (MHz) | 3 dB Bandwidth Typ. (MHz) | Stopbands I.L. > 20dB at MHz | Stopbands I.L. > 35dB at MHz |
|---|---|---|---|---|---|
| ★BP-10.7 | 10.7 | 9.6-11.5 | 8.9-12.7 | 7.5 & 15 | 0.6 & 50-1000 |
| ★BP-21.4 | 21.4 | 19.2-23.6 | 17.9-25.3 | 15.5 & 29 | 3.0 & 80-1000 |
| ★BP-30 | 30.0 | 27.0-33.0 | 25-35 | 22 & 40 | 3.2 & 99-1000 |
| ★BP-60 | 60.0 | 55.0-67.0 | 49.5-70.5 | 44 & 79 | 4.6 & 190-1000 |
| ★BP-70 | 70.0 | 63.0-77.0 | 68.0-82.0 | 51 & 94 | 6.0 & 193-1000 |

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

### Constant Impedance, 21.4 to 70MHz

| Model No. | Center Freq. MHz | Passband MHz loss < 1dB | Stopband loss > 20dB at MHz | VSWR 1.3:1 Total Band MHz |
|---|---|---|---|---|
| ★IF-21.4 | 21.4 | 18-25 | 1.3 & 150 | DC-220 |
| ★IF-30 | 30 | 25-35 | 1.9 & 210 | DC-330 |
| ★IF-40 | 42 | 35-49 | 2.6 & 300 | DC-400 |
| ★IF-50 | 50 | 41-58 | 3.1 & 350 | DC-440 |
| ★IF-60 | 60 | 50-70 | 3.8 & 400 | DC-500 |
| ★IF-70 | 70 | 58-82 | 4.4 & 490 | DC-550 |

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

NOTE: ★**Add Prefix P, B, N, or S for Pin, BNC, N, or SMA connector requirement.**

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F132 1-2 REVC

## Asian Center Opens For PowerPC Designs

A technical center for the design of PowerPC-based systems by Asian computer manufacturers has been opened in Taipei, Taiwan, by IBM and Motorola, both in Austin, Texas. The center will assist system developers, independent hardware and software vendors, and chipset suppliers with developing systems, subsystems and applications. Initially, it will support the Taiwan New PC Consortium, an organization created by the Computer and Communications Research Laboratories and the Taiwan Appliance Manufacturer's Assoc., and currently has over 31 computer companies developing hardware and software. First to release a PowerPC-based system from the consortium is Tatung, whose TPC-5510 supports Microsoft Windows NT, AIX, IBM OS/2, and Sun Solaris operating systems and operates at 66 or 80 MHz with a PowerPC 601 CPU. The machine comes in two form factors: one supports a CPU upgrade/level-2 cache socket, three PCI slots and five ISA slots; the other supports the upgrade socket but only two PCI slots and two ISA slots. Contact Motorola's Dean Mosley at (512) 891-2839, or IBM's Jim Smith at (914) 892-5389, and Tatung's Chris Hsu at (02) 592-5252 ext. 2418.

## Put 600-MHz IC PLL On 17-GHz-npn Gate Array

A novel mixed-signal process has been developed that will allow the fabrication of analog macros with 17-GHz npn transistors. Synergy, Santa Clara, Calif., has created a family of Analog macrocells that can be added to their ECL gate arrays. The arrays are based on the company's unique mixed-signal bipolar process, which builds trench isolated npn transistors sporting an $f_t$ of 17 GHz *(Electronic Design, May 2, p. 97)*. The MACROs include building blocks for building phase-locked-loops with operating frequencies ranging from 100 MHz to 2 GHz. These building blocks include phase detectors, phase-frequency detectors, variable delay elements, charge pumps and voltage-controlled oscillators (VCOs). One array user created a phase-locked loop and, with an assist from sophisticated frequency-domain techniques, measured phase jitter as low as 6.5 ps while running at 622 MHz. This may well be the lowest phase distortion yet reported. While the arrays are only available with npn transistors, a new version of the process carries a 7 GHz vertical pnp device. In addition, a biCMOS version of the process, with 1.2-μm CMOS, is also available. Other analog MACROs include 500-MHz 3-to-8-bit DACs, and glitchless 8-bit video DACs that are capable of driving a 50- or 75-Ω cable. For more information, call Kent Vandenberg at (408) 730-1313. *FG*

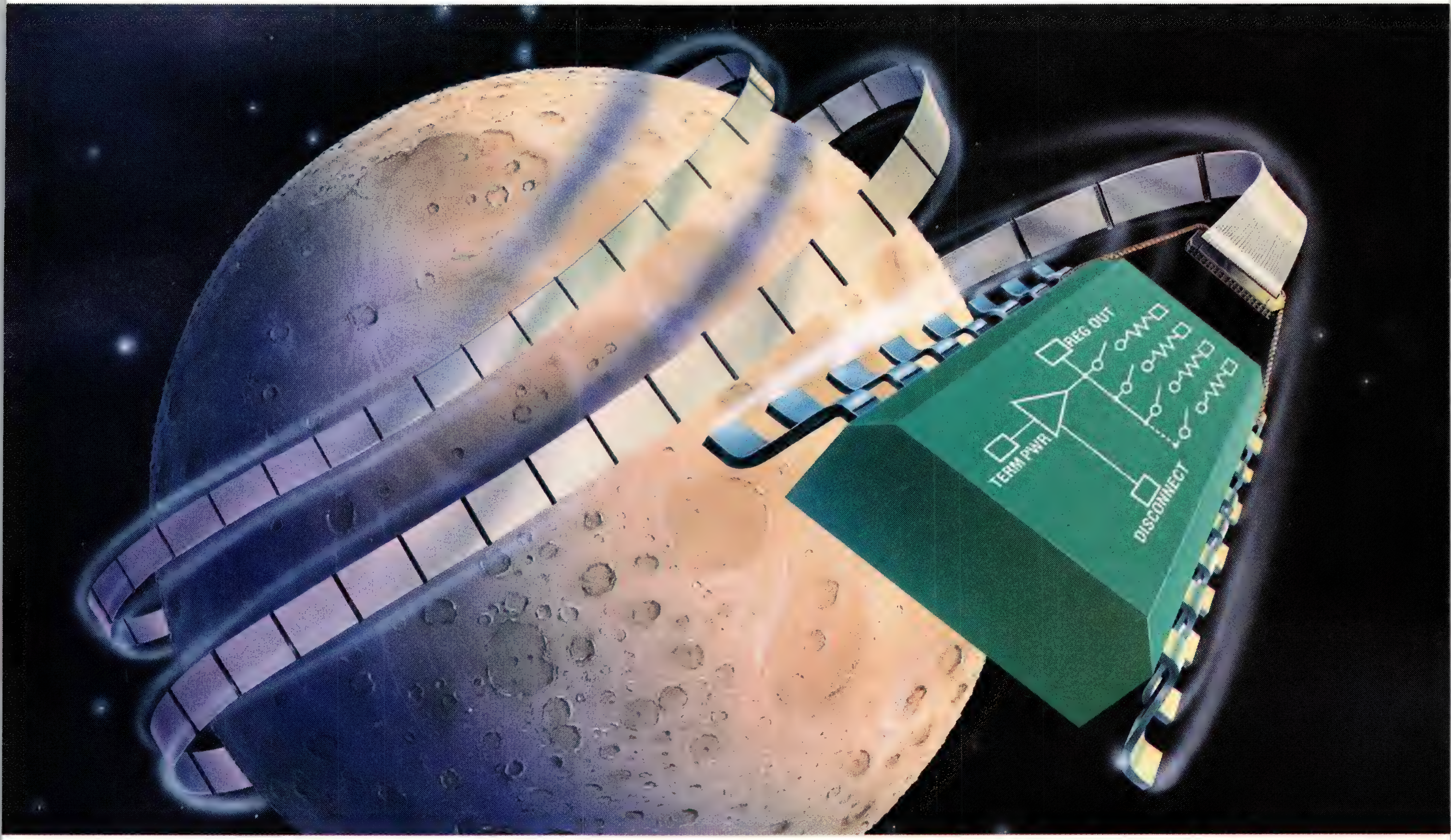
## Standards For Vocoder And Wireless Encryption

The Telecommunications Industry Association (TIA) has issued standards for two key technologies, a vocoder algorithm for digital cellular telephony, and a data-encryption protocol for use in land-mobile radio systems. The vocoder standard, issued as TIA/EIA IS-96, was designed to support the IS-95 spread-spectrum, code-division multiple-access (CDMA) standard, which was issued in July, 1993. The IS-96 standard establishes the technology for a variable-rate vocoder, which provides high-quality speech, using an average bit rate of 4 kbits/s. Entitled TIA/EIA/is-102.AAAA, the data-encryption standard (DES) was developed in conjunction with the Association of Public-Safety Communications Officials (APCO), as well as state and federal agencies. IS-102-.AAAA describes the encryption protocol for use in public-safety radio communications, such as police, fire and ambulances. Copies of either standard are available from Global Engineering Documents, Engelwood, Colo. Call (800) 854-7179. *LG*

## Convert Light To Digital Format

By converting light intensity directly into digital data, designers can build low-power equipment for such applications as environmental monitoring systems, color sensing, light reflection, and photographic exposure control. The TSL230, which is designed for portable and battery-operated microcontroller-based systems, consumes just 5 mW at 3 V and can operate from a 3- to 6-V supply. When not in use, the device from Texas Instruments, Dallas, can be switched to a power-down mode, where it draws just 10 μA. The device consists of a programmable photo diode and a current-to-frequency converter, which transforms the current output of the light-sensitive photodiode to a digital-compatible pulse train with a frequency that's proportional to the incident light intensity. The TSL230 converter's serial output can be connected directly to a microcontroller, DSP, or other digital-logic for processing. For information, call Texas Instruments at (800) 477-8924, ext. 4500. *RN*

# 3pF SCSI Gives Your Bus a Lift



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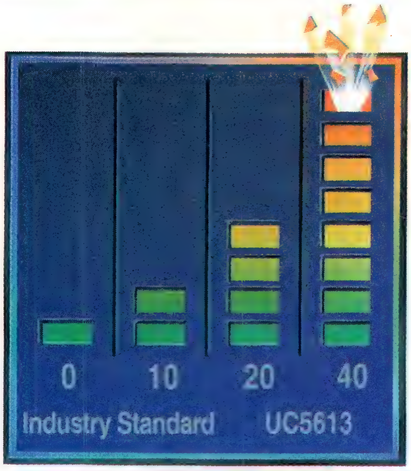

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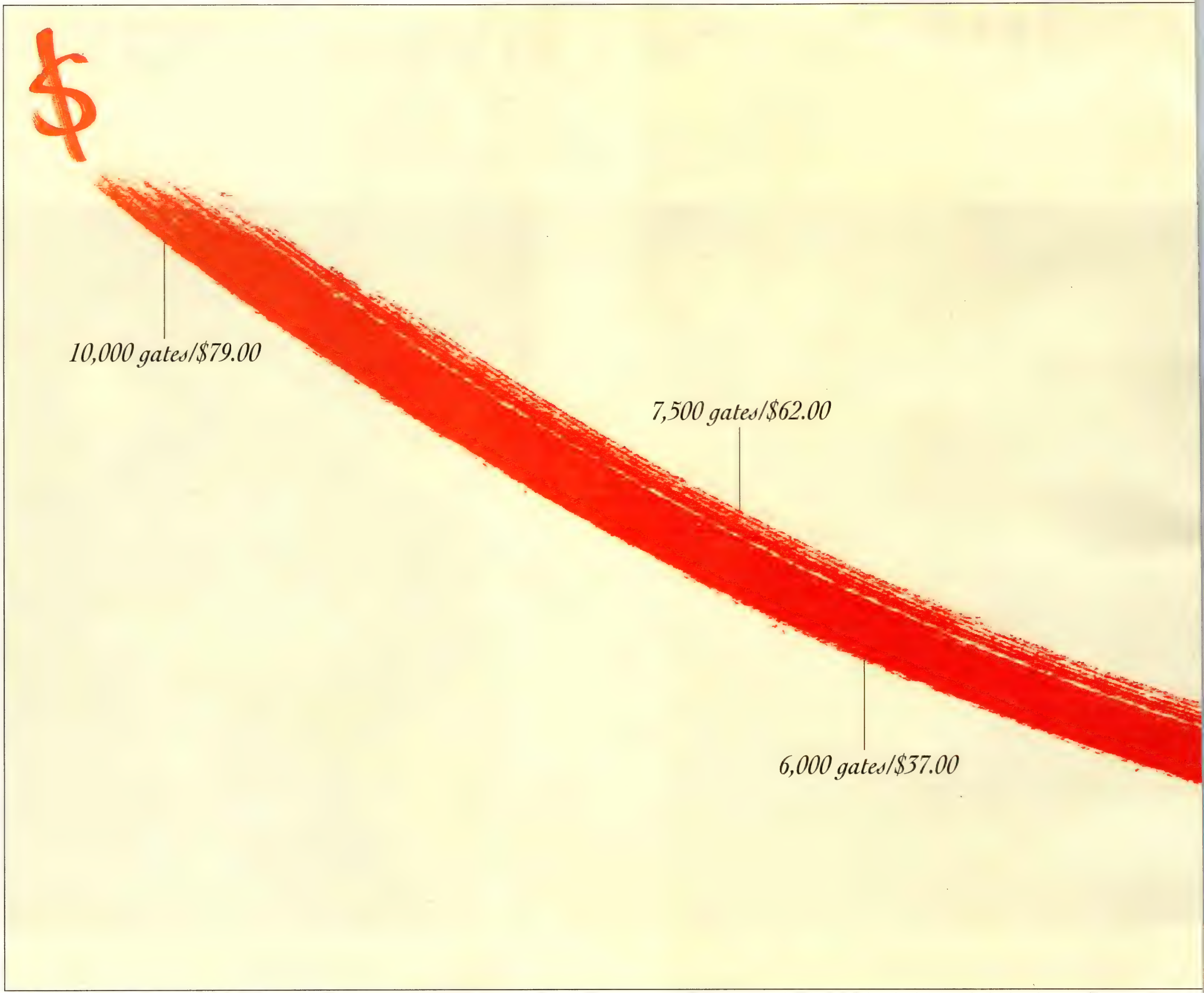

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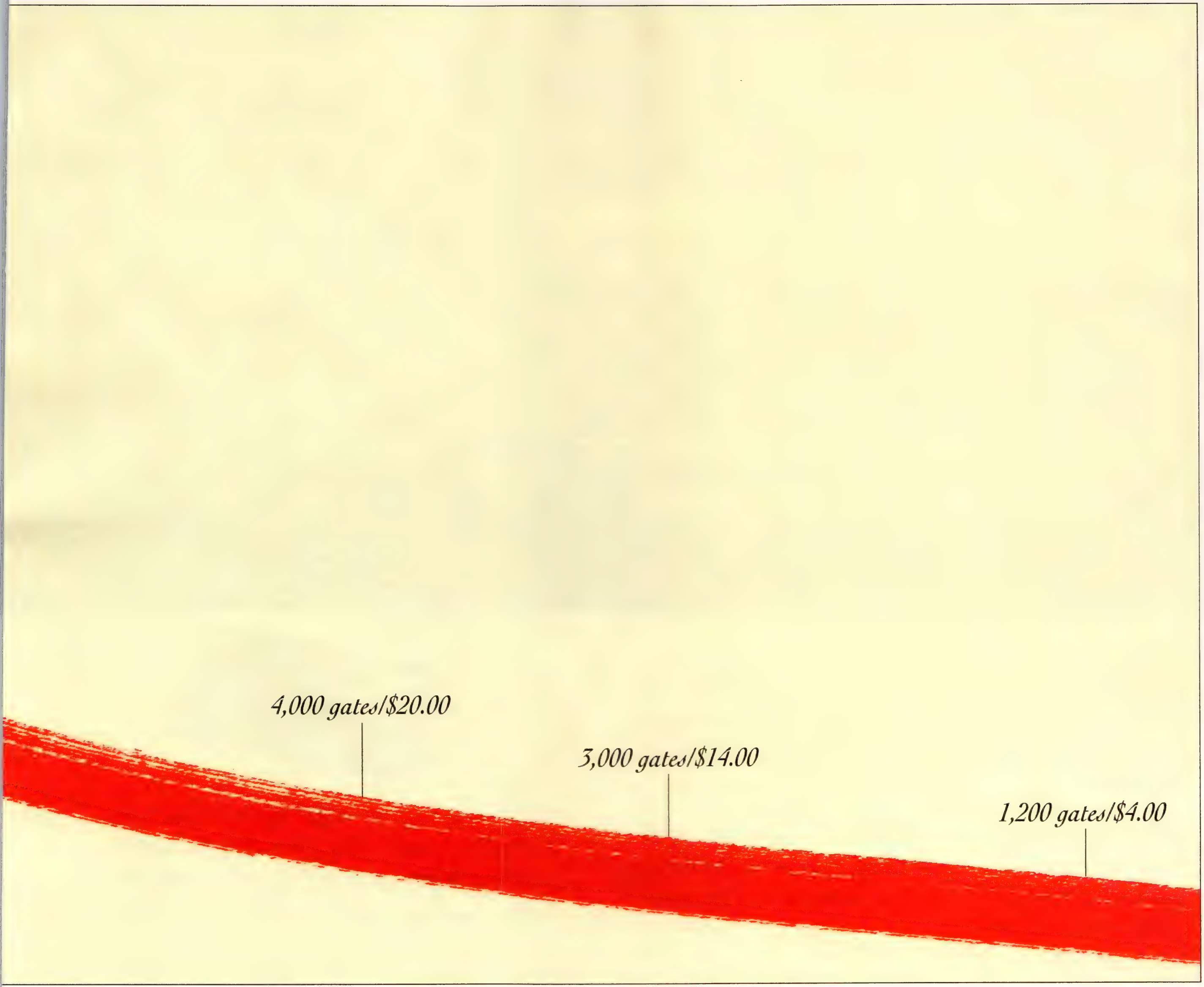

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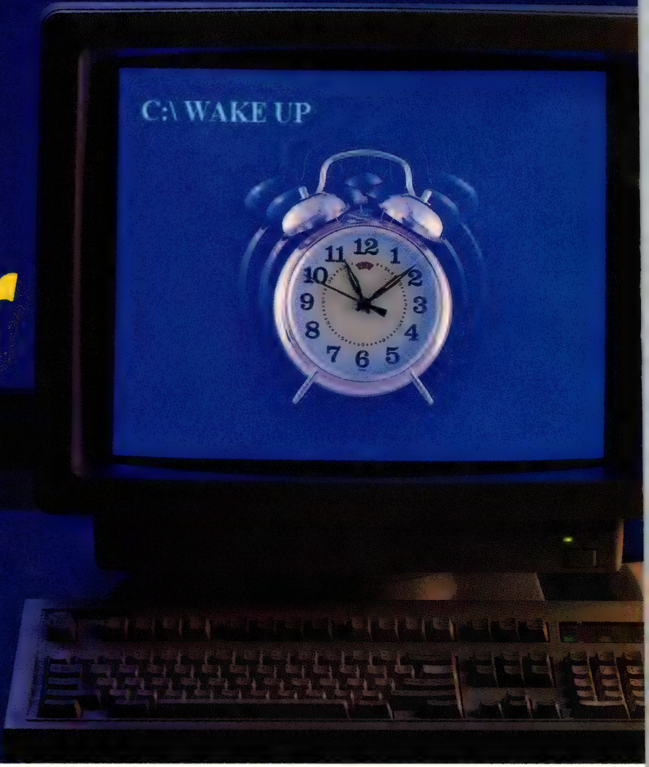

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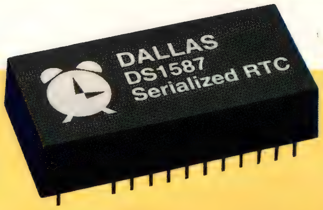

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# BIOS EMULATION SCHEME LETS RISC COMPUTER BOOT UP WITH PC GRAPHICS

The commoditization of workstations is posing an interesting challenge to system designers and system integrators when it comes to the graphics subsystem. Today, the broad array of performance choices and price points in graphics subsystems for PCs makes the integrator or user of RISC-based workstations more envious than ever before.

That envy stems from the very-restricted choice and very high prices associated with add-in graphics options usually available to the workstation. Choices are restricted because the graphics drivers and interface for a display subsystem typically must be custom written and optimized for that subsystem, which increases the amount of time needed to add a new card choice to the option list.

Ideally, it would be nice to get an already developed, attractively priced, off-the-shelf card for PC graphics and just be able to plug it into, say, a PCI-based motherboard in a RISC workstation, such as the one the Digital Equipment Corp., Marlboro, Mass., uses in its Alpha-CPU-based workstations. However, because the graphics cards typically contain a video BIOS written for x86-type microprocessors, they can't readily be used—until now.

A novel BIOS emulation scheme developed by DEC allows PC graphics cards with a standard video BIOS ROM to boot up in an Alpha workstation. In addition, the emulation scheme can be expanded to handle other I/O cards—disk-storage controllers, network adapters, and other functions can be moved directly from the PC to the workstation world without rewriting any software. DEC will provide this new emulation scheme to all of its Alpha system-development partners. Furthermore, DEC will even entertain licensing arrangements so that other suppliers of workstations not based on the Alpha processor can offer the ability to start up systems with PC add-in cards.

In a clone PC, option cards typically contain a BIOS extension ROM. The host-system BIOS then uses a well-established procedure in the motherboard BIOS to search for option ROMs to extend the BIOS. In a RISC PC, though, the code can't run directly. So the system firmware for the RISC machine must have code specifically built in for specific graphics cards. That restricts system designers, because they must preselect the graphics card support at the time they design and configure the system. This also delays the support of the latest card designs, creating a continuous upgrade problem.

With BIOS emulation, explains Peter Hayden, manager of BIOS compatibility software at DEC, the RISC machine behaves like a PC on startup and executes BIOS extension code in the emulation mode so that the system boots up just like a PC. Since the procedure only takes place during system boot, the time taken to set up and initialize the board is minimal. Thus, system performance isn't affected once the board is set up.

When power is turned on, the main system BIOS puts the RISC system into a PC emulation mode. As a result, the system emulates the way the PC goes out to look for extension ROMs, and then executes x86 code. Once the cards are recognized and the extension ROM code is executed, the system returns to its native RISC mode, but keeps all BIOS services for the PC cards.

Speaking in analogies, it's quite similar to the way a Basic interpreter works as opposed to a Basic compiler. Thus, each time a BIOS call comes in, the RISC machine interprets that call in real time just as if it were an x86-type processor. And in most cases, it does so without impacting performance.

The system BIOS can automatically detect x86 code and perform the cross-domain operations. Furthermore, most PC system BIOS functions can be mapped into RISC-system BIOS native-code functions. Consequently, the RISC machine can retain most of its characteristics and performance and avoid some of the performance losses typically encountered during emulation.

As an alternative, DEC's designers could have tried to just use a generic PC emulation scheme. However, because operations done at boot-up are different than when the computer runs application code, running a full PC emulation mode doesn't work. To detect the x86 video BIOS instructions, designers at DEC developed proprietary software that analyzes the instruction stream to detect the x86 commands.

Including an emulation technology adds some code to the RISC BIOS, but it's not significant in the overall scheme of things—just a few hundred kbytes of code. One more practical alternative to the BIOS emulation scheme is the OpenBoot approach, which is being implemented by Sun Microsystems and several PCI card suppliers. In the OpenBoot scheme, the video BIOS ROM contains multiple software images. The system then would access a particular preassigned address range to read in the native-code configuration information. The PCI specification defines how to search the BIOS ROM extension for the desired code image.

Another advantage of the BIOS emulation approach is that it keeps the amount of ROM on the add-in card smaller. It also allows use of ISA and EISA cards. OpenBoot only works for PCI-based cards without manual setup. Manually set jumpers on ISA and EISA cards would have to be used to set the CPU type. On top of that, emulation lets the system builder take advantage of all legacy cards—ISA, EISA, and possibly VL-Bus—as well as the new PCI cards. Thus, system designers and system users have a much broader choice of what can be plugged in.

Although the initial support focus is for graphics boards, the next likely target will be storage extensions, such as SCSI adapters. Relatively low-cost PCI-bus SCSI controllers make ideal candidates as add-in second control channels to the workstation. The extra channel can be used either for the purposes of redundant backup or as a dedicated channel for high-

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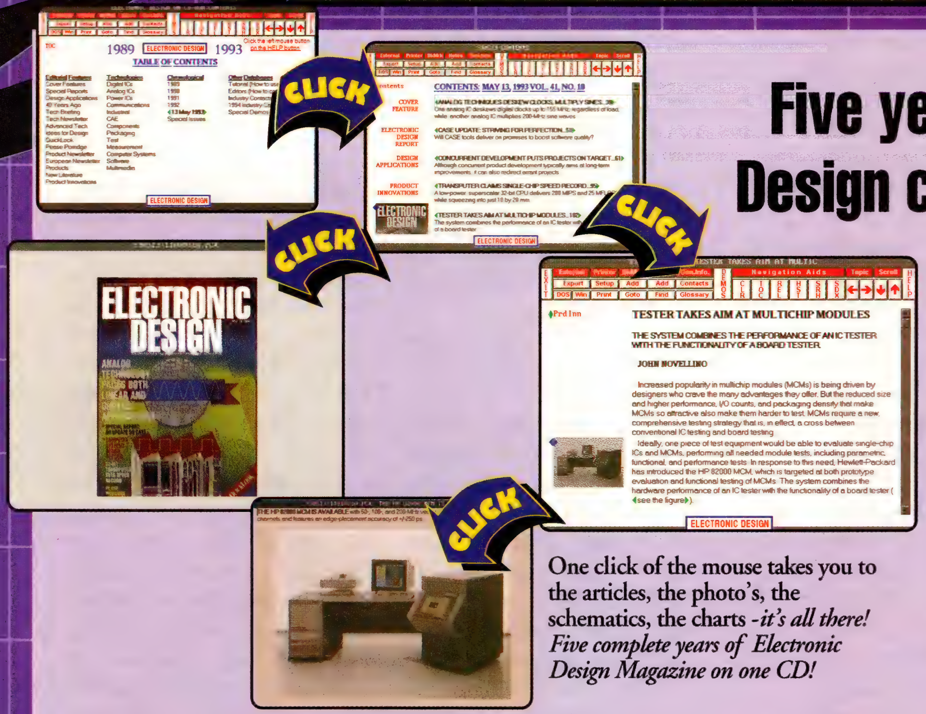

TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is being driven by designers who crave the many advantages they offer. But the reduced size and higher performance, I/O counts, and packaging density that make MCMs so attractive also make them harder to test. MCMs require a new, comprehensive testing strategy that is, in effect, a cross between conventional IC testing and board testing.

Ideally, one piece of test equipment would be able to evaluate single-chip ICs and MCMs, performing all needed module tests, including parametric, functional, and performance tests. In response to this need, Hewlett-Packard has introduced the HP 82000 MCM, which is targeted at both prototype evaluation and functional testing of MCMs. The system combines the hardware performance of an IC tester with the functionality of a board tester (see the figure).

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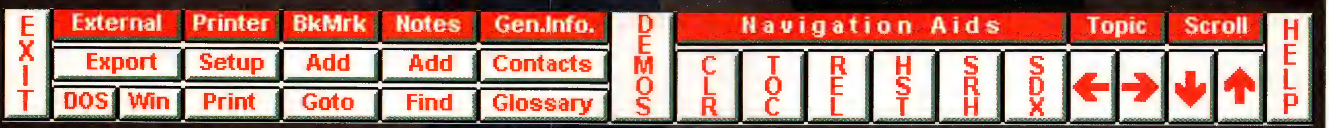

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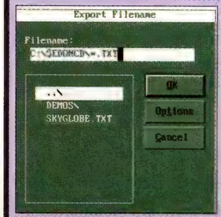

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The **Export** button will export any or all of an article based on your selection.

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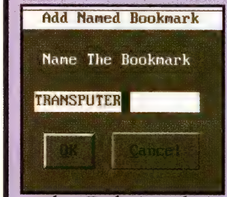

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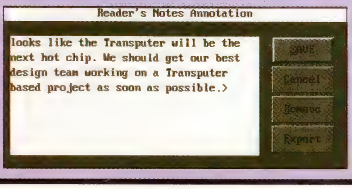

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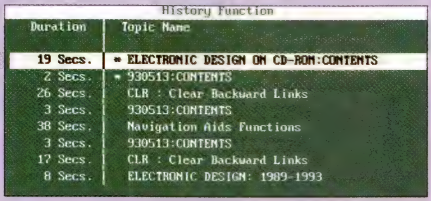

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  26 Secs.  |   CLR : Clear Backward Links
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   3 Secs.  |   930513:CONTENTS
  17 Secs.  |   CLR : Clear Backward Links
   8 Secs.  |   ELECTRONIC DESIGN: 1989-1993
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REL - *Show-Related Articles* - Calls up a list of, and lets you move to, related topics.

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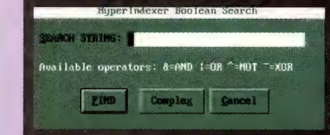

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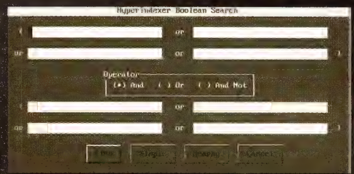

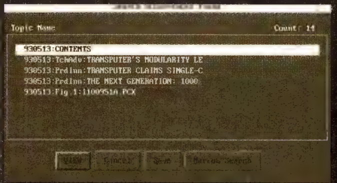

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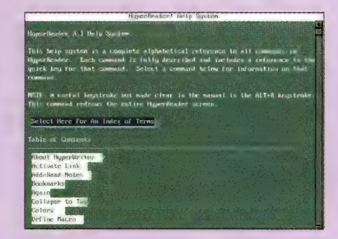

## MINIMUM SYSTEM REQUIREMENTS

- ☞ 80386 PC or better
- ☞ VGA video card adaptor w/640 x 480 pixel resolution 16 colors.
- ☞ 1 meg ram
- ☞ MS-DOS Version 3.1 or later

or low-speed peripherals. By dedicating a channel in such a manner, slow peripherals needn't bog down the main channel, which improves overall system performance.

As mentioned, the BIOS emulation software is free to Alpha customers—those who previously purchased the AXP-150 systems that run the NT operating system. The BIOS emulation software will be included in all upcoming Alpha/PCI systems.

System OEMs presently building Alpha systems also get the software free as part of a developer's package. They can replicate the code on each system without incurring any additional charge. The source code also has been licensed to American Megatrends Inc., Norcross, Ga. The company will create custom BIOS code that in turn will be licensed to system manufacturers.

For more information, contact Peter Hayden at (508) 486-2437.

*DAVE BURSKY*

# FUTURE PC DESIGNS DEMAND HIGH-SPEED I/OS, FAST GRAPHICS, AND LOW POWER

Three technical challenges dominate the world of personal-computer designers when planning next-generation systems: faster operation, lower power consumption, and, once attaining the other two challenges, improved features. These often diametrically opposed requirements are actually coming together as new I/O buses, higher-performance processors, better power-management techniques, and new graphics and multimedia circuits lay the foundations for the next generation of desktop and portable computers.

These demanding design areas will be addressed in the many technical papers, tutorials, and panel sessions at the Silicon Valley Personal Computer Design Conference and Exposition, July 27-29, at the Hyatt Hotel, San Jose, Calif. The focus will be on the latest CPU, bus, graphics, and power-management schemes, as well as key design issues.

One such issue involves moving data quickly within a computer or between a computer and peripherals, a critical factor in implementing high-performance computers as well as graphics and multimedia subsystems. Many papers at the conference will touch on this very topic, particularly when it concerns designing with local buses like the peripheral-component interconnect (PCI) bus, the Video-Equipment Standards Association (VESA) bus, the VESA media channel, and the high-speed P1394 bus. Other presentations will look at various I/O bus architectures, the use of isoEthernet for video conferencing, and the implementation of the technique of data streaming to move data quickly.

High-performance computing and graphics subsystems also will be spotlighted. Papers in various sessions will cover such issues as multiprocessor system design, designing with x86 and Power PC microprocessors, the optimization of clocking and skew to maximize system performance, and 3D graphics and multimedia implementation. Portable systems receive attention in sessions that cover 3-V/5-V system-interface issues, power-management techniques, PCMCIA modem and wireless LAN design, and infrared data links.

In the multimedia design track, designers at Rambus Inc., Mountain View, Calif., will examine how the VESA media channel and the PCI multimedia specification will impact the way graphics memory subsystems will have to be designed to ensure low-delay data transfers. I/O buses such as the 100-Mbit/s (extendible to 400 Mbits/s) P1394 standard will be analyzed by National Semiconductor Corp., Santa Clara, Calif., for use as multimedia interconnection schemes. National Semiconductor also will show how easily P1394 interfaces can be used on a system motherboard.

Four papers will explore multimedia and high-performance graphic displays. One paper from Weitek Corp., Sunnyvale, Calif., covers graphics acceleration and multimedia video. Another delivered by C-Cube Microsystems, Milpitas, Calif., goes into JPEG compression/decompression implementations. And, a pair of papers, one from 3DLabs, San Jose, Calif., and another from AT&T Microelectronics, Allentown, Pa., detail some of the first 3D graphics adapter-card designs.

Designers manipulating 3D graphics information, if they're not careful, can end up eating up all of the host CPU's processing power. To ensure against that happening, the AT&T Microelectronics presentation will show how to take advantage of pixel-embedded control bits. In addition, a multimedia panel session on Wednesday, July 27, examines the impact of next-generation games on a PC's architecture. The session will focus on such topics as graphics memory architec-

## GET STARTED ON THE RIGHT FOOT

Foundation tutorials at the conference also will cover five key topics—The ABCs of multimedia technology; issues and approaches to designing mixed 3-V/5-V systems; implementing I/O device interfaces with the Access.bus; designing PowerPC systems using the Reference Platform specification; and dealing with Plug and Play issues when using PCI and PCMCIA buses and peripherals.

Supporting the foundation presentations will be daily keynote speeches that will probe into the future challenges. Keynotes include design challenges for usable multimedia systems by Dr. Alexandre Balkanski, a vice president at C-Cube Microsystems, Milpitas, Calif.; low-power computing design challenges by Dr. Mark Horowitz, a professor at Stanford University, in Calif.; and extending the reach of the PCI bus by Ron Smith, general manager of Intel's PCI Div., Santa Clara, Calif.

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tures, data-movement approaches, and accelerated drawing.

A full view of all portable-system design issues is planned for Thursday, July 28. Presentations by Microchip Technology Inc, Chandler, Ariz.; Geoworks Inc., Alameda, Calif.; and Crystal Semiconductor Inc., Austin, Texas, will look at three key aspects of portable systems: intelligent battery management, operating-system design considerations, and infrared data-link implementations (including the standardization efforts of the InfraRed Data Association), respectively.

Power-management techniques for keyboards also will be the focus of a presentation by Hitachi America Ltd., Brisbane, Calif. In addition, Elpac Power Systems, Irvine, Calif., will concentrate on portable-system design considerations for batteries, battery chargers, and power supplies.

The use of PCMCIA cards in portable systems is the key to flexibility and upgradability in many subnotebook and personal digital assistants. In that respect, the implementation of a wireless LAN adapter and the shoehorning of a 28.8-kbit/s modem into PCMCIA formats will be themes of a pair of papers from two divisions of AT&T Global Information Solutions, one based in Duluth, Ga., and the other in Huntington Beach, Calif., respectively.

Low-power level-shifting issues will be examined by Texas Instruments Inc., Dallas. Discussed are the pros and cons of split-rail (dual 3.3- and 5-V supplies) as well as 5-V-tolerant pure 3.3-V interfaces. Mixed-signal design issues in portable hardware also is key to well-behaved hardware. To that end, Crystal Semiconductor, Austin, Texas, will address mixed-signal needs in PDAs and other portable systems. And, how to implement a video subsystem that PDAs and other portable systems can use without draining large amounts of battery power will be detailed by VLSI Technology Inc., Tempe, Ariz.

PCMCIA implementations for memory and I/O functions also will be covered on Thursday July 28, in a presentation by M-Systems Inc., Tel-Aviv, Israel, while the use of flash file systems and flash memories is addressed by Adtron Corp., Fremont, Calif. Rounding out the Thursday presentations will be a panel session that examines the issues of merging multimedia technology into portable system formats. The panel will be chaired by Western Digital Corp., Irvine, Calif.

For performance fanatics, the presentations on Friday, July 29, will satiate the needs of some high-performance system designers. Plug and Play system designs as well as PCI interface designs will be central topics of presentations by Cirrus Logic Inc., Fremont, Calif.; LSI Logic Corp., Milpitas, Calif.; and National Semiconductor. High-performance modular architectures, multiprocessing systems, and several PowerPC system implementation papers will provide glimpses of systems to be released this year and next.

Cyrix Corp., Richardson, Texas, for example, will describe a multiprocessor architecture based on its forthcoming M1 superscalar x86-compatible processor, while Wyse Technologies Inc., San Jose, Calif., will present details on the design of highly modular hardware that can be quickly and easily be upgraded. Not to be left out, Intel Corp., Santa Clara, will show how Energy-Star compliance can be designed into Pentium-based systems.

PowerPC system design will be covered in a trio of papers from Motorola Inc. and IBM Corp., both in Austin, Texas. Discussion on system design issues involving clocking and skew margins is expected from TriQuint Semiconductor, Santa Clara, Calif. In addition, level-2 cache design will be covered by Integrated Device Technology Inc., Santa Clara, Calif.

Wrapping up the final day is a panel session that will examine the speed advantages and implementation issues associated with various existing and forthcoming I/O buses. Chaired by TriQuint Semiconductor, the session will cover topics such as the P1394 bus, IBM's SSA (serial storage architecture), the scalable coherent interface, and the PCI bus.

*DAVE BURSKY*

### WANT TO GO?

The 1994 Silicon Valley Personal Computer Design Conference and Exposition takes place at the San Jose Hyatt Hotel, San Jose, Calif., July 27-29. Registration at the door is $295 per day or $550 for all three days. Contact Sys-Tech Research, San Jose, at: (408) 293-8383 (telephone); (408) 293-0901 (fax); or 71147.1000@compuserve.com (e-mail).

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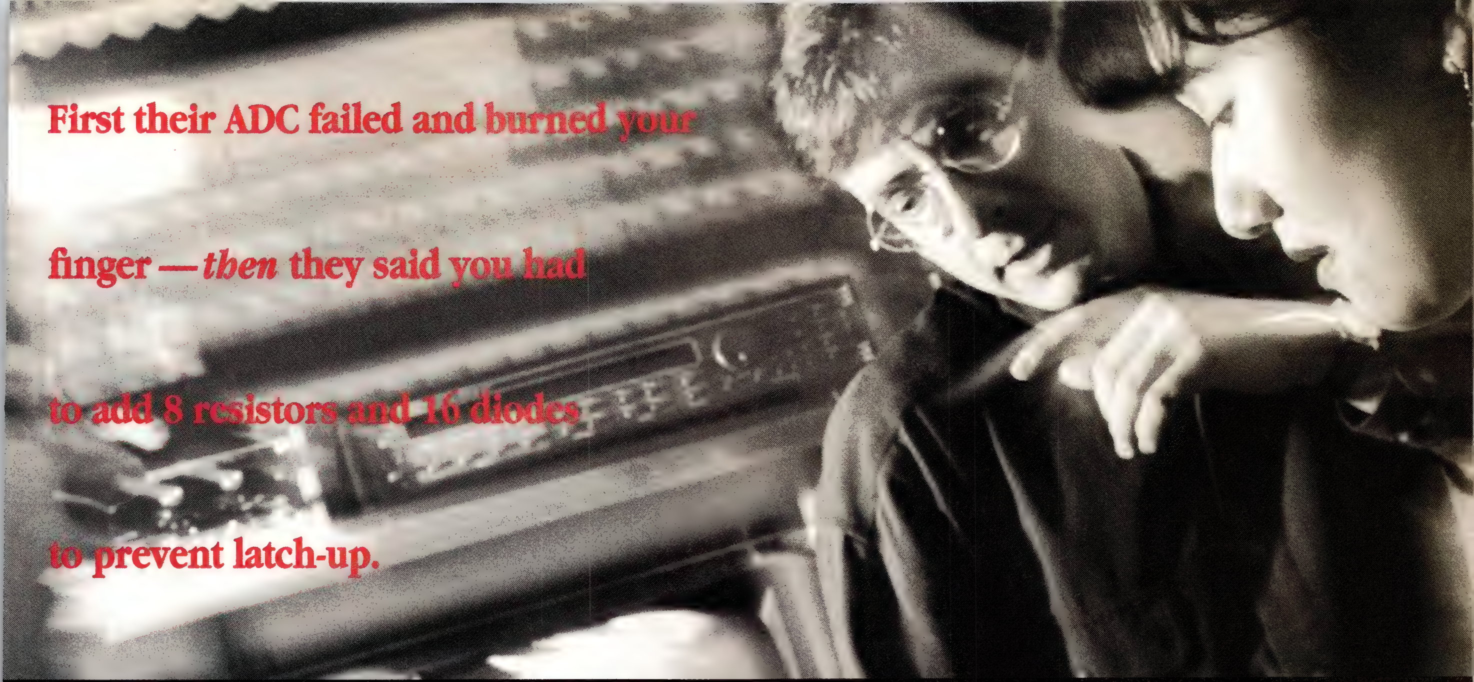
# 64-BIT BUS HANDLES 533 MBYTES/S IN HIGH-END MULTIPROCESSOR SYSTEMS

The high clock rates typifying the latest round of microprocessors require a very high-speed bus to handle data flow between system resources. Recently developed local buses like the PCI transfer data at a maximum rate of 133 Mbytes/s, which may suffice for a uniprocessor system. But, when multiple CPUs are combined in a system, the bus can become a data bottleneck.

To eliminate that bottleneck, designers at Vitesse Semiconductor, Camarillo, Calif., came up with a new concept called the V-Bus. The V-Bus, which features a sustained data-transfer rate of 533 Mbytes/s when operating at a clock frequency of 66 MHz, is built with a symmetric multiprocessing architecture. It gives all of the bus masters the same authority to use system resources, such as memory and other I/Os. Although multiple CPUs can be manipulating the data, the V-Bus supplies a way to maintain data coherency. And the bus is processor-independent, meaning that it works with most architectures.

The V-Bus is a 64-bit data bus with a 40-bit demultiplexed address bus. It can operate at a maximum



First their ADC failed and burned your finger — *then* they said you had to add 8 resistors and 16 diodes to prevent latch-up.

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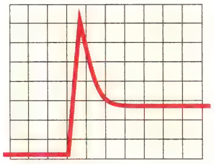

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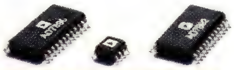

| SPECIFICATION | AD7890 | AD7893 | AD7892 |
|---|---|---|---|
| Throughput (ksps) | 100 | 117 | 500 |
| Channels | 8 | 1 | 1 |
| Power Dissipation | 30 mW | 25 mW | 60 mW |
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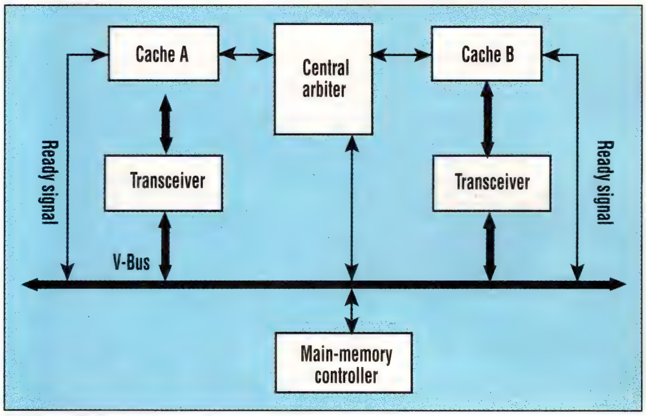


speed of 66 MHz using Gunning transistor logic (GTL) or at 50 MHz with TTL. It supports the MESI memory protocol to maintain memory-data coherency. To reduce snoop latency, two tag RAMs are used: one is dedicated to CPU accesses and the other services the snoops.

To improve snoop latency, the V-Bus supports a line-lock mechanism. Only the line that corresponds to the locked-cycle's address will be locked. If there are no long-latency I/O devices on the bus, then a locked cycle that needs to use the V-Bus will wait for outstanding bus cycles to complete their data phases before being locked.

To maintain software compatibility, the V-Bus doesn't impose any particular scheme for address mapping. This allows those OEMs using the V-Bus to choose their own method of caching, write protection, and memory-mapped I/O. In turn, it helps prevent unnecessary address translation from one memory space to another.

The V-Bus architecture requires an interface chip or external cache, equipped with the V-Bus protocols, to isolate the CPU from the V-Bus. The CPU's speed can differ from the V-Bus' speed because the external cache is decoupled. Consequently, CPUs can be upgraded without affecting the V-Bus interface.

The cache controller has to convert the CPUs to the common V-Bus speed. The actual cache memory can be a direct-mapped or set-associative type, but must accept burst bus transfers for both read and write operations.

On the multiprocessing bus, any task can execute on any CPU, and a task started on one CPU can be shifted to another. The bus will handle the data coherency as well as balance the workload.

Up to eight electrical loads are supported. These can be CPU-cache modules, memory, I/O devices, or I/O bridges.

The minimum space between elements is 1.5 in. By decoding the bus-cycle definition, each element on the bus must be able to determine whether a given cycle belongs to them. Each node then responds by floating or driving the Ready signal *(see the figure)*. The bus' only limitations are determined by the scalability of the software, and CPU and cache performance.

The V-Bus connector, which is a 200-pin microstrip vertical plug, is available from Amp Inc., Harrisburg, Pa. (part number AMP121354-9). Its dimensions are 4.95 by 0.648 by 0.285 in.

For more information on the V-Bus, contact Vitesse Semiconductor at (408) 730-3653.

*RICHARD NASS*

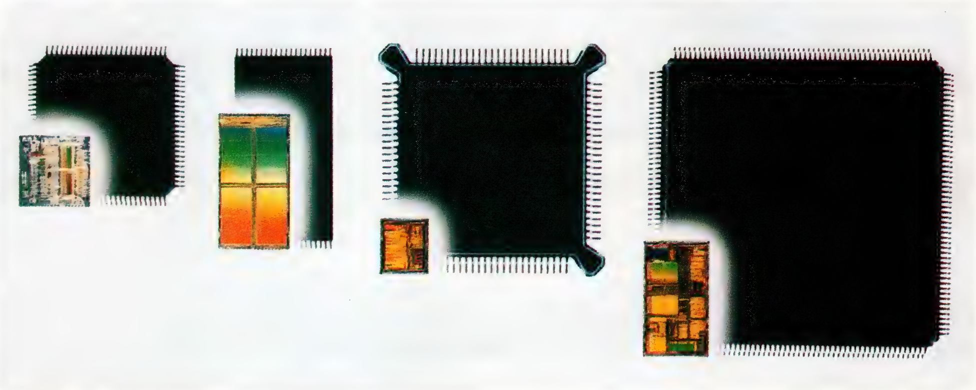
# BARE KNOWN-GOOD DIE NOW AVAILABLE ON A LARGE SCALE

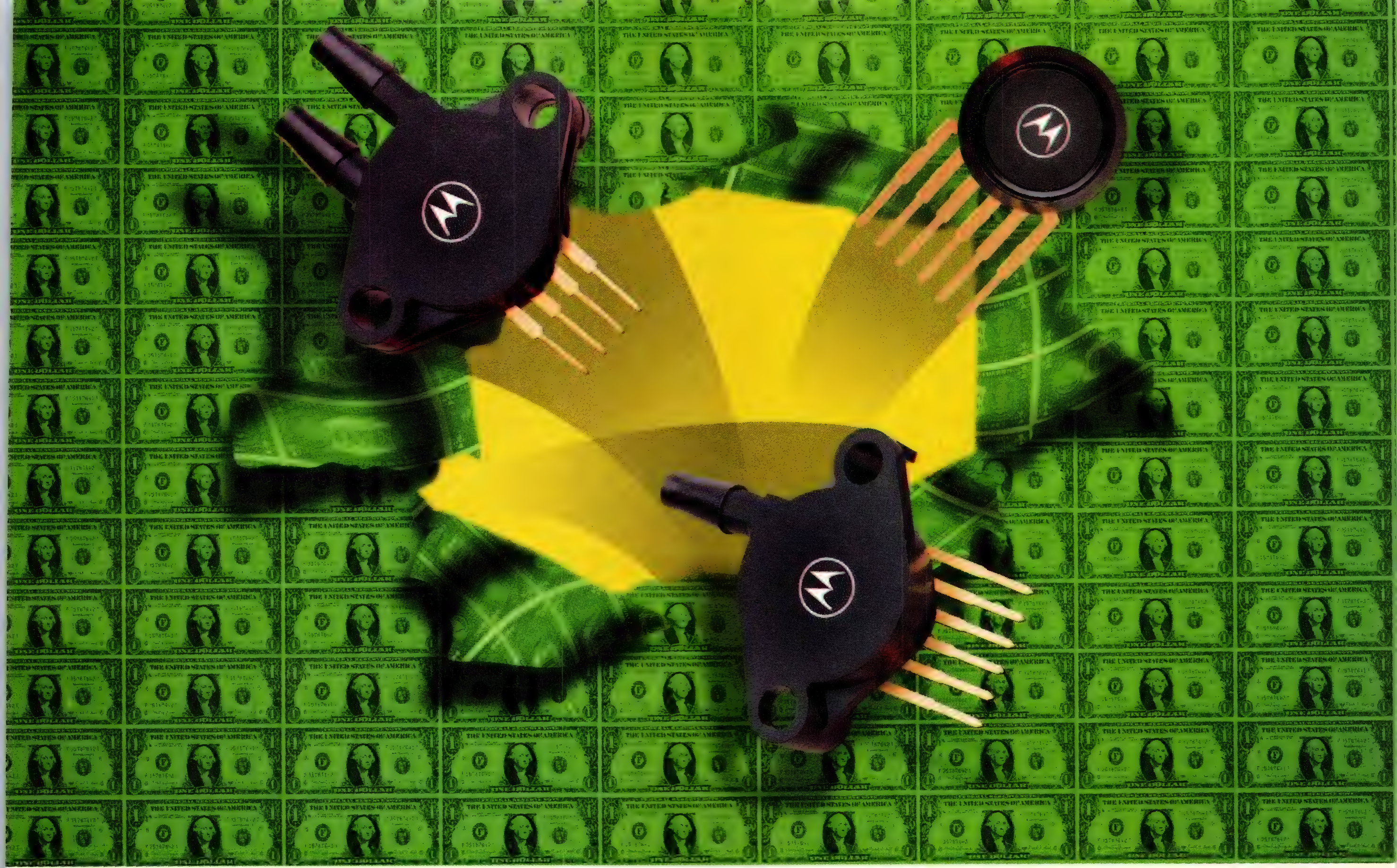
It's no secret that the multichip-module (MCM) industry will get off the ground only if semiconductor makers finally solve the puzzle of supplying products as known-good bare die. Now, with the announcement of its SmartDie products, Intel, Santa Clara, Calif., has given MCMs their biggest boost in some time. Thanks to a die-level burn-in process and a technical-alliance program involving various assembly subcontractors, Intel can offer bare-die versions of processors and flash memories. Eventually, the SmartDie program will encompass the Pentium and i960 CPUs.

Many emerging system applications, including embedded PCs, PCMCIA cards, handheld systems, and personal communication devices, are presenting designers with form-factor constraints that were previously unimaginable. With much of the growth in die consumption driven by such applications, it's clear that the time for bare die has arrived.

In most cases, packaged CPUs and memories are simply too bulky for applications like PCMCIA cards. For example, the bare-die version of the 33-MHz 386CX CPU takes up only 12% of the area of the packaged version and 25% of the height. Intel says up to 5-to-1 gains in overall pc-board real-estate savings are possible with bare die compared with packaged counterparts *(see the photo)*. This means designers can place the same functionality in a much tighter space, or much more functionality in the same space.

A number of enabling technologies must fall into





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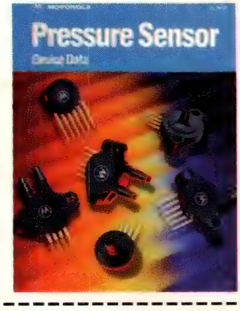

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line for bare die to be practical. First and foremost are solutions for at-speed testing, burn-in, and handling. Intel developed the capability to test die products to levels equivalent to traditional packaged ICs. The die are tested to operate over the full commercial-temperature range (0 to 80°C), including full-speed testing of parametrics.

Intel's die-level burn-in process uses the DieMate system from MicroModule Systems (MMS), Cupertino, Calif., and TI's Materials and Controls Group, Attleboro, Mass. DieMate involves a carrier/socket system that requires no die post-processing. Intel is the first semiconductor manufacturer to use DieMate in production.

Handling of bare die is, quite literally, a sensitive issue. Intel's solution is to ship the die in Gel-Paks, which are vacuum-release trays produced by Vichem Corp., Sunnyvale, Calif. The trays enable the capture and removal of contaminants, afford convenient die storage and retrieval, and provide surface and edge protection. The trays are packaged in moisture-barrier bags for further protection. Intel is currently evaluating tape-and-reel options for the future.

While just being able to procure bare die clears a major OEM design hurdle, figuring out how to deal with them also is a daunting obstacle. Intel has lined up die-level manufacturing assistance for customers through its Technical Alliance Program (TAP), bringing assembly subcontractors into the fold. The companies, which include MMS, Anam/Amkor, Jabil Circuit, SCI Systems, S-MOS Systems, Solectron, and Valtronic USA., offer bare-die users technical support in designing and assembling die into small equipment.

Call Intel at (800) 626-7256.

*DAVID MALINIAK*

## 40-MBYTE/S SERIAL LINK POSES AS AN ALTERNATIVE TO SCSI

The Small Computer Systems Interface (SCSI) has proven quite popular with computer designers. Yet it carries some unwanted baggage, such as different software standards that can cause conflicts. As a result, system designers sometimes seek alternatives when connecting storage subsystems like disk drives and disk-drive arrays.

One alternative that's getting more notice is the Serial Storage Architecture (SSA), developed by IBM, San Jose, Calif. Many companies have endorsed the SSA_AMP, Conner Peripherals, Interphase, Ironics, ITT Canon, Micropolis, NCR, QLogic, Siemens-

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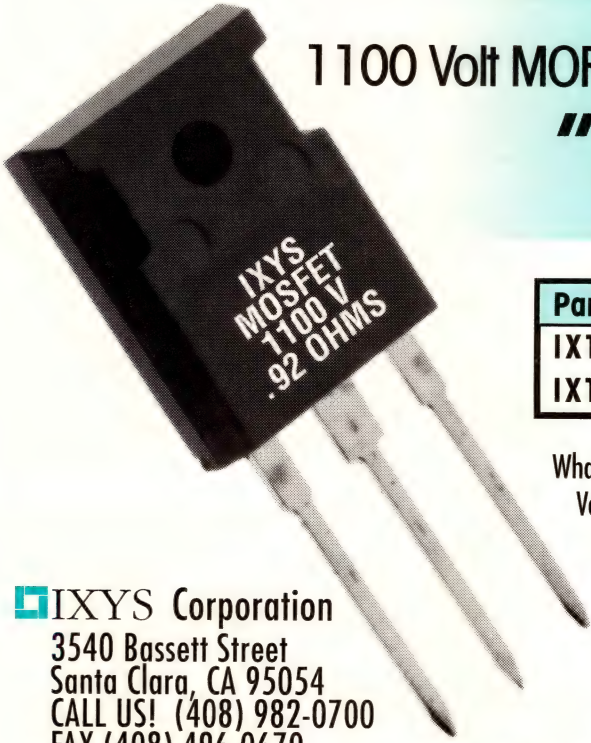

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Nixdorf, VLSI Technology, and Western Digital.

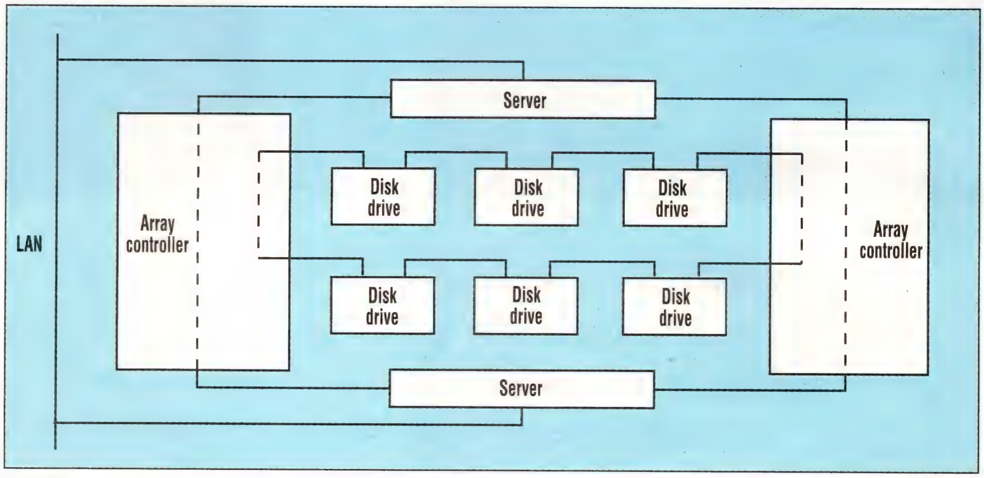
The SSA bus' serial architecture eliminates problems of SCSI-connection large cables. It requires no discrete terminators or address switches. Moreover, its serial-connection ASICs are less complex and require fewer pins than those chips used in the SCSI bus, reducing cost.

Because one data signal is used on the SSA bus, there's no clock skew to consider as the data rate or cable length increase. The bus' copper-wire transmission rate is 20 Mbytes/s in each direction (40 Mbytes/s total), for a maximum cable length of 10 m (1 km over fiber optics using a small form-factor connector). The SSA's high bandwidth, low protocol overhead, and short frame length help maintain responsiveness and throughput under high loads.

The SSA bus uses a two-signal connection for full-duplex operation. It employs a self-clocking code. The data clock is recovered from the data signal itself, rather than being transmitted as a separate signal.

For copper wire, the SSA bus uses the differential-pair method, requiring four wires. The shielded cable has a diameter of under 6 mm. The bus calls for external microminiature nine-pin D-shell connectors. Internally, twisted-pair or flex cable is employed.

SSA's flexible addressing scheme facilitates strings, loops, switched loops, or cyclic paths, as well as hot plugging. Up to 127 devices can be connected per string or loop. In a dual-loop configuration, the outer loop



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**Now available, the first fully compliant 1394 chipset from TI.** We're providing breakthrough silicon in this emerging interface standard. And we are the first to offer a physical-layer chip (TSB11C01) and a link-layer chip (TSB12C01). Combined, they give you a full-chipset solution.

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- Single connector for all applications
- Compliant with proposed 1394 standard

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**Inventing the future: You, Texas Instruments and 1394.** New possibilities are what the 1394 standard is all about. For complete product specification, phone your nearest TI office (listed below).

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connects the servers to the array controllers, while the inner loop connects the controllers with the storage devices *(see the figure)*.

The SSA specification is made up of two components: SSA-PH and SSA-SCSI. SSA-PH covers the physical-transport layer_ the physical and electrical specification of the serial link. SSA-SCSI is the SCSI-2 mapping layer. Because the logical aspects of the SCSI specification are appropriate for addressing serially-attached peripherals, SSA-SCSI was carried over to the SSA specification in the physical mapping of the interface.Designers can thus port their products from SCSI to SSA with minimum code rewriting (typically about 15%). In addition, similar mappings for the SCSI-3 bus will be provided when that specification is approved byANSI.

Each SSA node performs extensive error checking and transparent frame recovery. When the devices are configured in a loop, alternate paths to each device ensure that no single point of failure exists.

ANSI formed the X3T9.7 Committee to approve the SSA standard. During that time, IBM designed the Serial Interface Chip (SIC) that implements the SSA protocol. The part currently is being sampled.

IBM also offers an evaluation card, a protocol analyzer, and a 2-Gbyte disk drive. Full microcode listings also are also available.

Call IBM's SSA Project Office at (408) 284-6039.

*RICHARD NASS*

## LATE-BREAKING DEVELOPMENTS...

**Lab work seen as key to better engineering education...**To reflect what it feels are the real-world needs of engineering graduates, Drexel University revamped its undergraduate engineering curriculum. The traditional theoretical curriculum has been replaced with laboratory-based, problem solving for teaching engineering fundamentals. Starting in September, first- and second-year students will spend at least three hours a week in the Philadelphia school's new high-tech engineering lab. Most engineering schools focus on theoretical math and science courses for the first two years, says Drexel engineering professor Robert Quinn. After completing the theory classes, students move on to hands-on engineering courses. Drexel's approach emphasizes practical engineering instruction from the outset, says Quinn. After their first year, the students will alternate six-month periods of cooperative work experience with on-campus learning. Drexel built a state-of-the-art facility to house two 15-station labs equipped with 150 pieces of equipment from Hewlett-Packard.The effort is funded in part by a five-year, $2.1 million NSF grant. Drexel's work is the lead project in a 10-institution, $4.5 million research effort to improve undergraduate-engineering education quality in the U.S. *JN*

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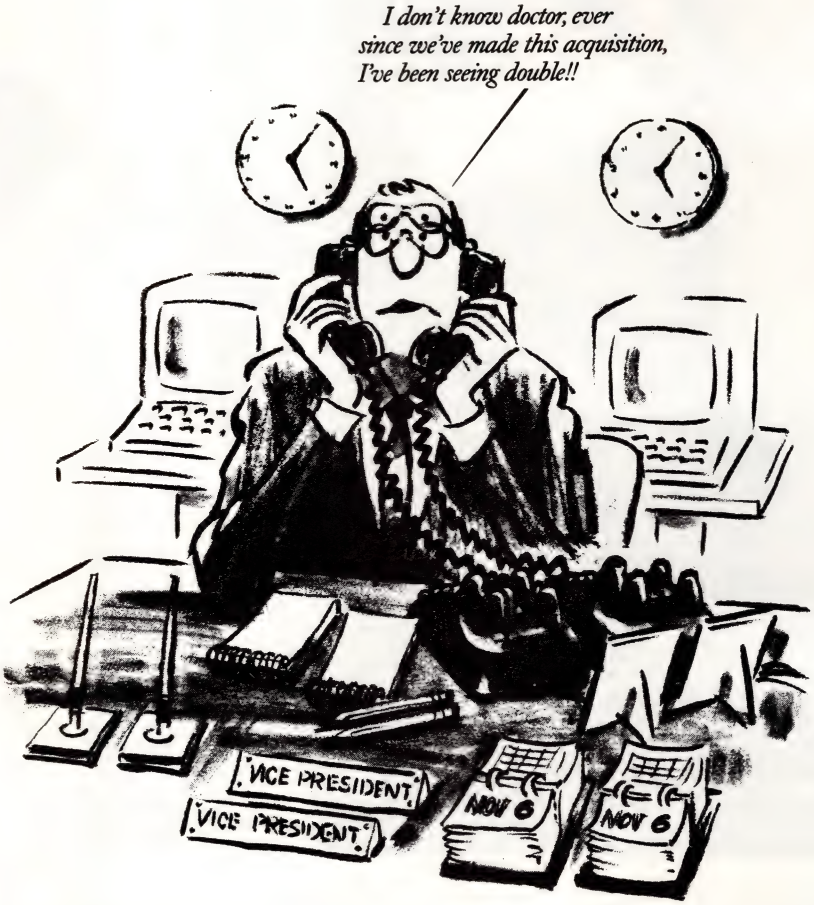
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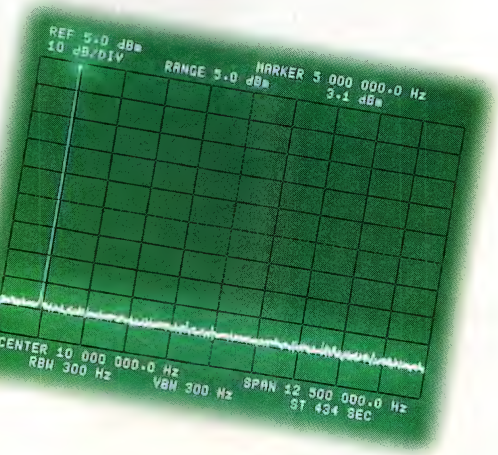

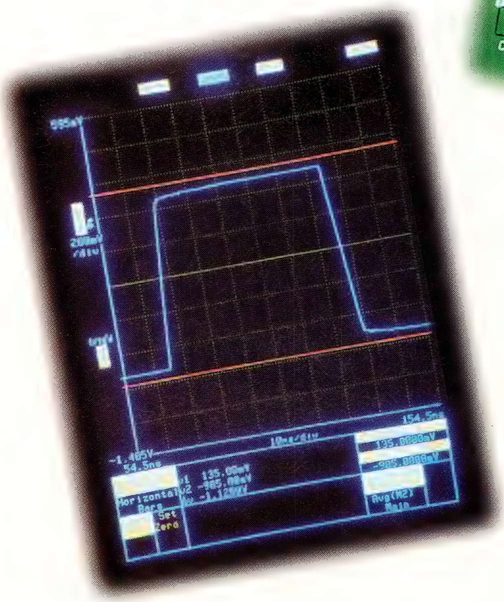

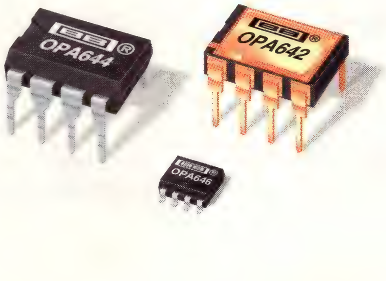

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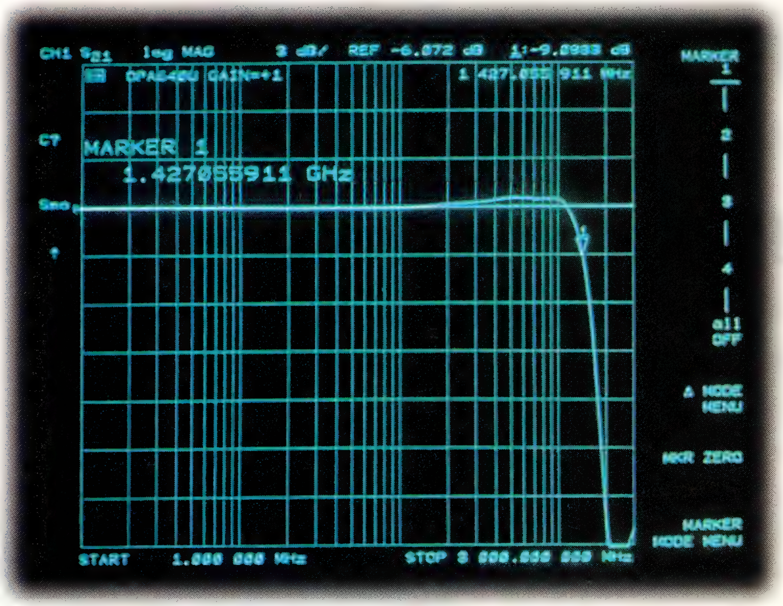

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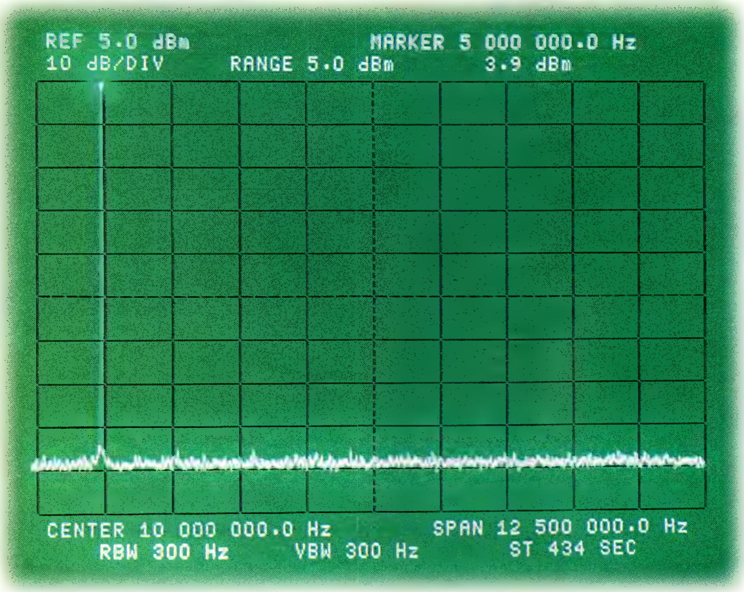

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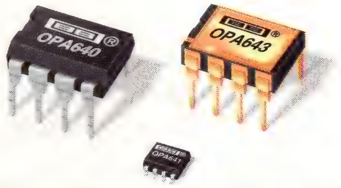

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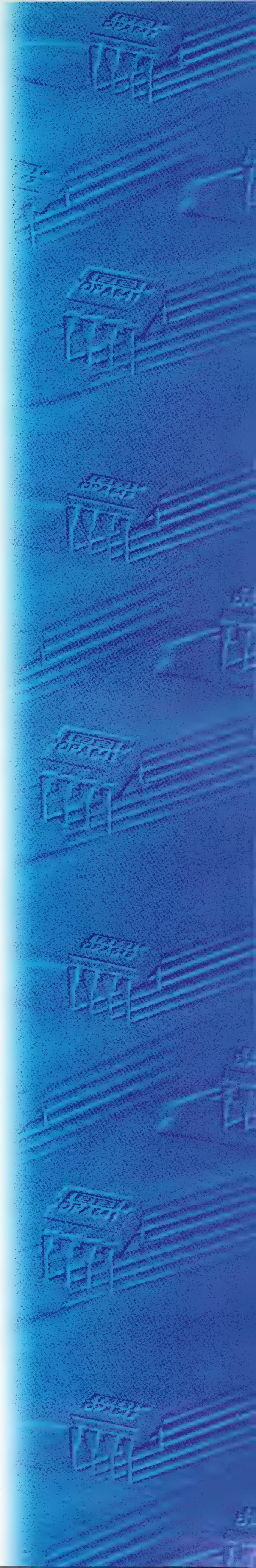

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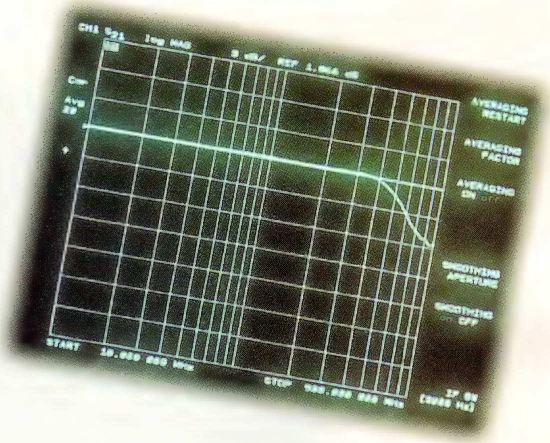

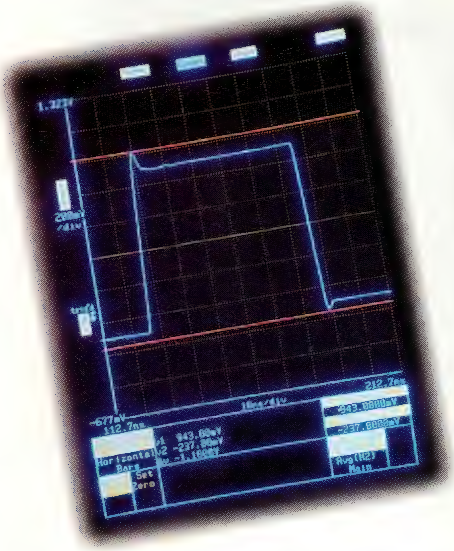

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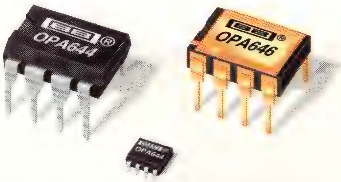

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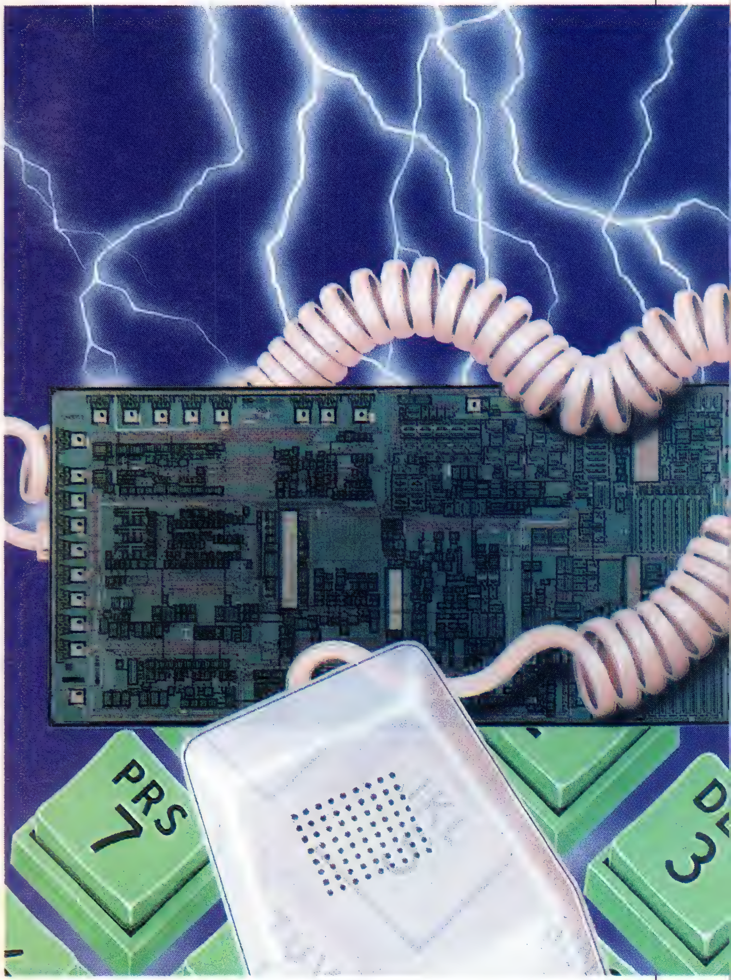
### HIGH-VOLTAGE BONDED-WAFER ICS CREATE FIRST SLIC TO SWITCH THE 93-V RMS PHONE-LINE RING VOLTAGE ON-CHIP, ELIMINATING PABX RELAYS.

# SLIC EJECTS RELAYS FROM PABX LINE CARDS

**FRANK GOODENOUGH**

As telephone private-area branch exchanges (PABXs) become common fixtures within even the smallest businesses, the demand grows for lower-cost and smaller-size PABX systems. PABX systems interface to a telephone company's central-office (CO) switch via subscriber-line interface circuits (SLICs). These SLICs reside on line cards, located in both the CO and the PABX, and must handle the harsh environment of the telephone network, including high "ring" voltages, transients, and lightning.

The traditional approach in dealing with these tasks has been to use expensive and bulky relays on the line card. However, a recent SLIC development from Harris Semiconductor will completely undo that procedure. The company devised a bonded-wafer process that allows them to put the ringing function, which requires switching 93 V rms, on one SLIC. On top of that, two such SLICs are incorporated in one tiny package—a plastic 80-pin metric quad flat pack (MQFP) that measures 14 by 20 mm. This is the first commercial IC to be built on a high-voltage bonded-wafer process.



Harris' HC-5506 SLIC is located on a line card in a PABX and provides an interface between the harsh environment of the telephone line's twisted-pair wiring and the low-voltage voice-signal-processing circuits. It detects the subscriber's "off-hook" events (such as picking up and hanging up the telephone), relays dial pulses and dual-tone multifrequency (DTMF) tones to the PABX CO circuits, and alerts the subscriber to the presence of an incoming call by applying the high-voltage ac ringing signal directly to the twisted-pair lines. As a result, it provides two channels of transparent communication between the voice-signal-processing circuits on the line card and the twisted-pair telephone line.

In developing the HC-5506 SLIC, Harris, the first "volume" producer of bonded-wafer analog ICs, moved a bonded-wafer process that created near-gigahertz-bandwidth low-voltage op amps to a process that produces high-voltage ICs. The double-metal-layer bonded-wafer process replaced a conventional single-metal, high-voltage, dielectrically isolated (DI) process that's been employed to build SLIC products for over 10 years.

A bonded wafer's narrow oxide-filled trenches, reaching from the surface of a die to the buried oxide layer, make possible very dense high-voltage devices. This results in smaller die (about 30% smaller using an earlier single-metal bonded-wafer process) than those produced from conventional DI processes *(see "High-voltage IC process," p. 58).*

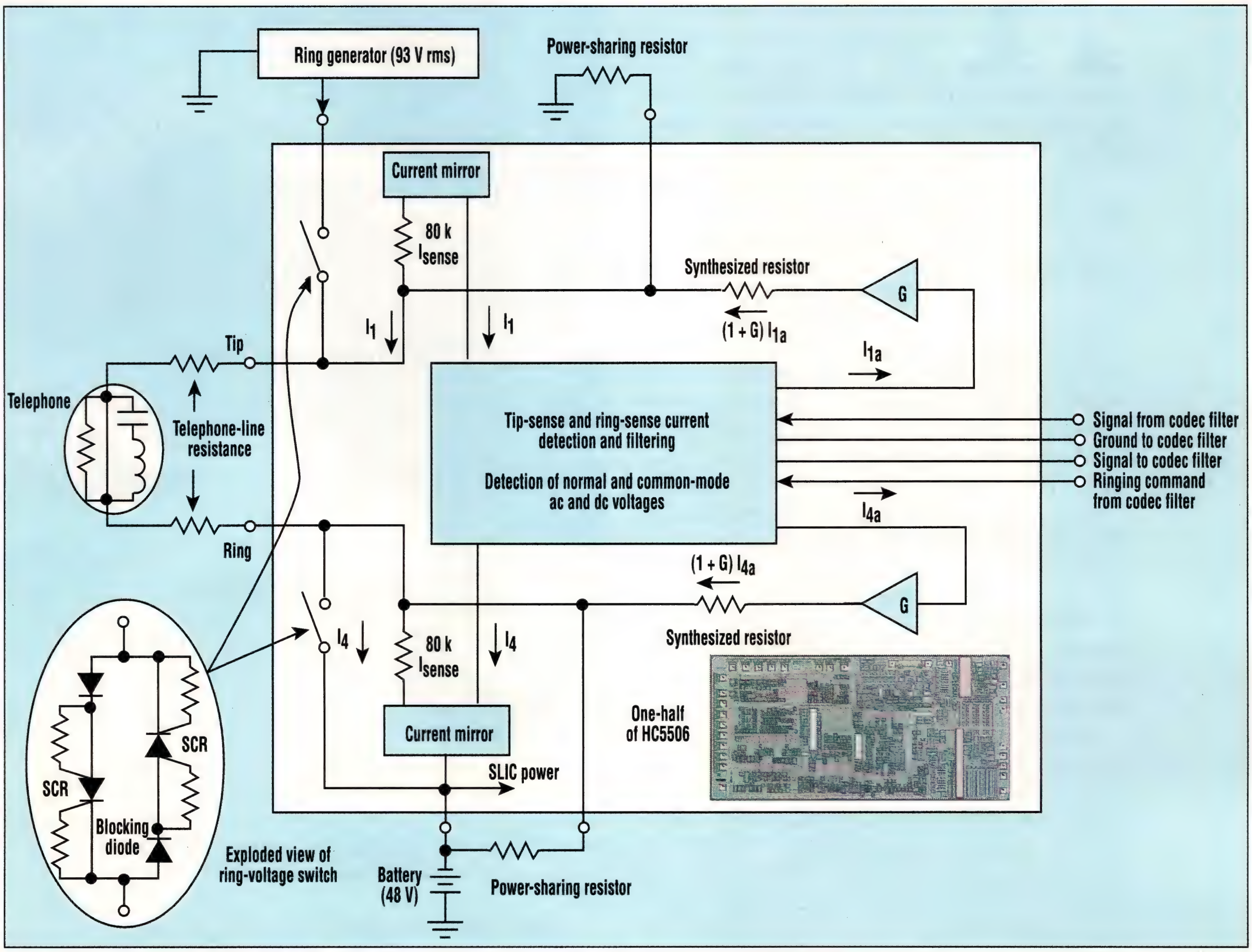
Getting the two die into the tiny package also required coming up with a pair of novel patented circuits. These circuits reduced each SLIC's power-dissipation level to under 500 mW *(Figs. 1 and 2).*

The HC-5506 not only is the first commercial SLIC to incorporate the ringing function, it's also the first high-voltage bonded-wafer IC designed completely "from scratch" and the first to incorporate double-level metal. Adding ringing to the die eliminates a pair of Form C (single-pole double-throw) electromechanical relays from the line card. And because the density of the process allowed two SLICs to be crammed onto the HC-5506 die, adding ringing eliminates two relays from the card *(see "I thought BORSCHT was beet soup?," p. 62).*

## A TALL ORDER

To understand the significance of the new HC-5506 SLIC, one needs to examine the "tall order" of functions handled by a telephone line card. Line cards perform what in telephone-company lingo is known as the BORSCHT functions:

- ***Battery feed,*** which provides dc power for the telephone at the end of the line.
- ***Overvoltage protection,*** which protects the SLIC and the PABX or CO exchange from high-voltage transients such as lightning strikes.
- ***Ringing,*** which provides a signal to ring the telephone.
- ***Supervision,*** which detects service requests. For example, it detects when a telephone is picked up so a call can be made and when someone hangs up the telephone.
- ***Coding,*** which digitizes the signals going from the telephone to the CO, and converts the digital signals coming from the CO to the telephone (or from another telephone) to analog form.
- ***Hybrid,*** which combines incoming as well as outgoing telephone analog signals.



**1. THIS SOLID-STATE SLIC** incorporates a pair of 250-V switches built from SCRs and diodes. The Harris HC5506 SLIC replaces the electromechanical relays now used to switch the ringing voltage (93 V rms) to the telephone line.

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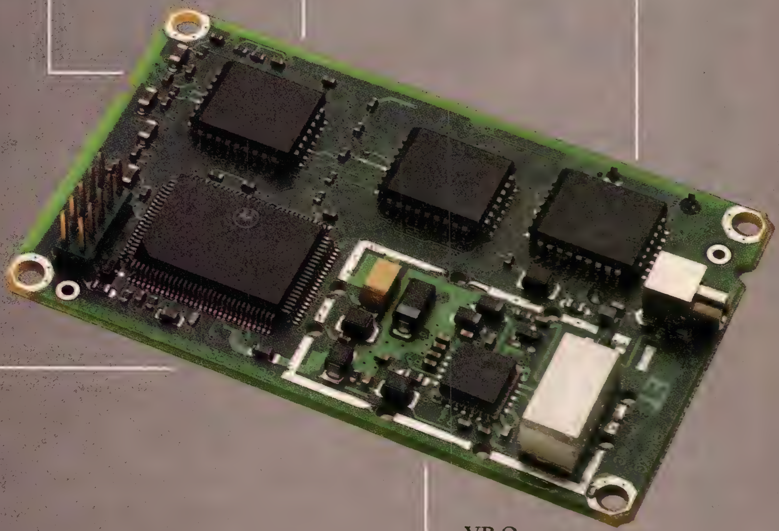

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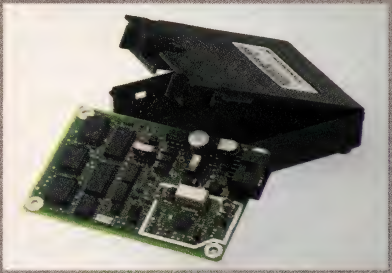

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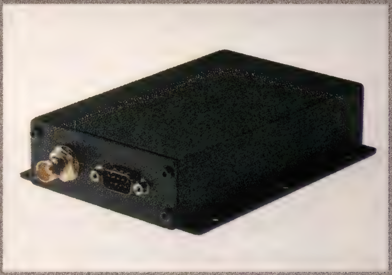

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- ***Test***, which permits checking the telephone line for faults.

To handle these functions, many of the line cards in today's PABX systems still require several chips, as well as a number of off-chip devices, including discrete transistors, relays, and passives (transformers, resistors, and capacitors). The chips include early solid-state SLICs and an audio codec and a filter (or a Codec-filter called a "combo").

No SLIC is currently available that can perform all of the BORSCHT functions. However, Harris and others have successfully integrated the battery feed and hybrid functions (and to some degree the supervision and test functions) on single chips. Some of these ICs employ polysilicon-handle DI to create the high-voltage circuits required by these functions, while others employ transformers and complex anti-saturation circuits.

The HC-5506 SLIC's development was driven by two major factors: cost and size. Putting two SLICs on one chip and eliminating the relays (the latter can cost as much as $1 each) reduces both of those factors and saves on valuable pc-board area. Furthermore, because the relays are significantly thicker than the SLIC'S 80-pin MQFP, the cards can be placed closer together. In addition, the largest external capacitor required by the SLIC is just 0.2 µF in value, permitting surface-mount construction. Thus, a given-sized PABX can handle more lines, or its package can be reduced in size. Both cut the cost per input telephone line. Harris estimates that a PABX supplier can save 33% on component costs per telephone line by eliminating the relays and using half as many pc boards.

## RING ON CHIP

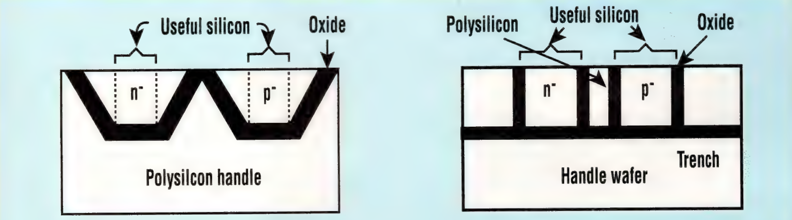
Integrating the SCRs that perform the ringing function also provides precision-timed, inherent zero-current switching, and increases system reliability. At the same time, it reduces the high-voltage transients that cause crosstalk between pairs in cable groups. Low crosstalk is becoming important now that low-level digital signals in the Integrated Services Digital Network (ISDN) co-

## HIGH-VOLTAGE IC PROCESS

The Harris SLIC process represents the first high-voltage production bonded-wafer process ever developed. Much like the conventional dielectric-isolation (DI) processes it replaces, the SLIC provides the ability to galvanically isolate individual transistors, or groups of transistors, from each other in tubs or islands with bottoms and side walls of silicon dioxide. The alternative, the more common junction isolation (JI) process, employs walls formed by back-biased pn junctions.

A DI process, often referred to as a silicon-on-insulator (SOI) process, offers major advantages to telecommunications ICs such as SLICs, which must handle high voltages and interface with the harsh environment of the real world. SOI processes eliminate the pn junction and its parasitic SCR that can cause latch-ups during power-up, during hot-board insertion, or when induced transients come off the Tip and Ring lines from the telephone.

The troublesome pn junction contains a depletion layer. It extends into the "isolated" island and must be separated from the depletion layer forming the base-collector junction within the island. These depletion layers are large, particularly at the high voltages seen by SLICs, mandating that the space between devices in adjacent islands be twice as wide in ICs built on JI processes as those built on SOI processes. In addition, the pn junction must be reverse-biased at all times to maintain isolation. Therefore, the isolated region must be tied to a voltage that's more negative than any point in the circuit. ICs built on DI processes don't suffer these constraints due to the layer of silicon dioxide surrounding active and/or passive devices. They can partake of voltages above and below the power-supply rails without disrupting the chip.



Conventional polysilicon-handle SOI process

Bonded-wafer SOI process

Having successfully built SLICs on what's called polysilicon-handle DI (developed by Harris over ten years ago when it was known as Radiation Inc.), why did Harris move to bonded-wafer SOI for the HC5506 SLIC? One reason is that the new process will allow the move from 4- to 5- or 6-in. wafers. Conventional DI processing is limited to 4-in. wafers, and die size is significantly reduced. The narrow, vertical trenches (used for isolation), with their oxide-coated walls, are provided by bonded wafers. The trenched tubs waste less silicon area than the sloped walls of the oxide-lined tubs used in conventional DI processes *(see the figure)*. The near-vertical trenches (borrowed from DRAM technology) are formed by reactive-ion etching (RIE). After etching, the walls are oxidized and the space between them is filled with polysilicon.

The workhorse transistors available to designers using the high-voltage process built on the bonded wafers consist of complementary 80-V npn and pnp devices with betas of 400 and 110, respectively, and Early voltages of 120 exist in cable groups with analog subscriber lines.

Like most devices for telecommunication applications, SLICs must meet a variety of domestic and international standards, from wire to complete systems, to remain compatible with a technology that's over 100 years old. It must appear as a pair of wires like the relays, transformers, and other passive components that it replaces, which—at least theoretically—were perfect. As a result, the HC-5506's data sheet contains over 100 specifications defining its performance under particular operating conditions. Most of these are provided as minimum or maximum specifications.

The HC-5506 features a maximum $V_{TIP} - V_{RING}$ residual feedthrough of –33 dBm (or –75 dB relative to 93 V rms). The $V_{TIP} - V_{RING}$ residual feedthrough can be considered the ringing-voltage feedthrough to the line when the HC-5506's solid-state "Tip" and "Ring" switches are open *(Fig. 1, again)*. The ringing voltage is 93 V rms over a frequency range of 22 to 54 Hz. Because 0 dBm is defined as 0.775 V rms across 600 Ω, and –33 dB below 0.775 V equals 17 mV rms, then the ratio of 93 V to 17 mV is approximately 5454:1 (about 75 dB). Thus, the feedthrough of the ringing voltage to an operating telephone line, across the open switches, is 75 dB below 93 V rms.

and 140. Their $f_t$s run 300 and 60 MHz, respectively. The process also allows the building of vertical npn and lateral pnp transistors rated at 250 V. However, their $f_t$s are limited to 12 and 9 MHz, respectively, while operating with 20 V between collector and emitter. These $f_t$s will drop to 5 and 2 MHz with 5 V between collector and emitter. The 250-V devices are used to build the SCRs and the output stage of the transconductance amplifiers.

The 80-V transistors form the remainder of the amplifiers and the other analog circuits in the SLIC while the logic is handled by 10-V Schottky diodes. One major challenge hurdled by the SLIC's design team was to come up with a closed-loop amplifier possessing a gain-bandwidth product of better than 1 MHz. They wound up using the 250-V output transistors with an operating frequency response (if providing gain) of less than the amplifiers' required gain-bandwidth product. That is, the transistors' $f_t$s are a function of their collector currents and their collector-emitter voltages. While the peak $f_t$ might be 9 MHz, operating $f_t$ can be as low as 300 kHz for the output-stage devices under various SLIC operating modes and different loads.

The preceding paragraph illustrates well the often confusing jargon of "plain old telephone system," commonly referred to as POTS, which developed over the years on its own. For example, the terms Tip and Ring are the names given the two wires of the twisted pair between the subscriber's telephone and the line card—but they *both* carry the ringing voltage between SLIC and the telephone. However, the *ring generator* (which develops the ringing voltage) is usually connected to the Tip wire, while the Ring wire is connected to the battery. In the days of switchboards with their plugs and jacks, the Tip and Ring wires were connected to the tip of the plug and the metallic ring contact behind it, respectively.

## POWER LIMITING

Maximum power dissipated by each HC-5506 SLIC is 500 mW, 1 W total for the chip. However, each SLIC must limit the dc line current from the 48-V battery (which powers the telephone) to 30 mA. The worst-case condition occurs when powering what's called a "short loop." It occurs when the 200- to 400-Ω telephone is very close to the PABX. If the telephone is just a few feet from the PABX line, resistance may be only a few ohms. But the battery's full 48 V is required because it may have to drive several miles of twisted-pair line, such as when a PABX services a large multi-building factory, hospital, or university campus. The SLIC must be able to put at least 16 mA into 1800 Ω.

Under short-loop conditions, the load current, limited by the SLIC to 30 mA, drops only 6 V across a potential 200-Ω telephone load (modern electronic telephones tend to have the lowest resistances). The remaining voltage (42 V) must be dropped across the SLIC. A 30-mA current would dissipate about 1.26 W/SLIC, which represents over 2 W of package power dissipation. Novel circuits within the SLIC keep power dissipation below 500 mW/SLIC, or less than 1 W for the HC-5506's plastic MQFP (its conservative specification states 1.1 W total power dissipation).

Minimum longitudinal balance for the HC-5506 SLIC between 200 and 1000 Hz is 58 dB. Longitudinal balance is telephone jargon for the SLIC's common-mode-rejection ratio when handling a telephone's signals on the twisted-pair telephone line. Crosstalk between the two SLICs within the package is a maximum of –85 dB.

Other specifications for the HC-5506 SLIC include a maximum signal swing between transmit and recieve modes of 2.18 V p-p, maximum on-hook ringing current of 75 mA peak, and maximum off-hook ringing current of 105 mA peak. Minimum line leakage from tip to ground, ring to ground, and tip to ring is 30 kΩ.

The SLIC has a loop resistance when the battery voltage is between –42 and –58 V of 200 to 1800 Ω during the non-dialing phase, and 0 to 1800 Ω during the dialing phase. The dc loop current is a minimum of 16 mA, at a line resistance of 1800 Ω and with the battery voltage set at –42 V and the SLIC's $V_{CC}$ at 4.75 V. Typical dc loop current is 30 mA.

Still other specifications include a maximum of 2% zero-crossing distortion (ringing on-hook). The SLIC's ring-trip comparator threshold level is 10 mA typical.

While designed for PABX rather than CO line cards, the HC-5506 offers a number of programmable features. These include gain and impedance matching, which may make it adaptable for CO applications in some countries (particularly developing or underdeveloped countries like China and even India). Other chip features include a Tip and Ring open state, two-wire ac and dc loop-

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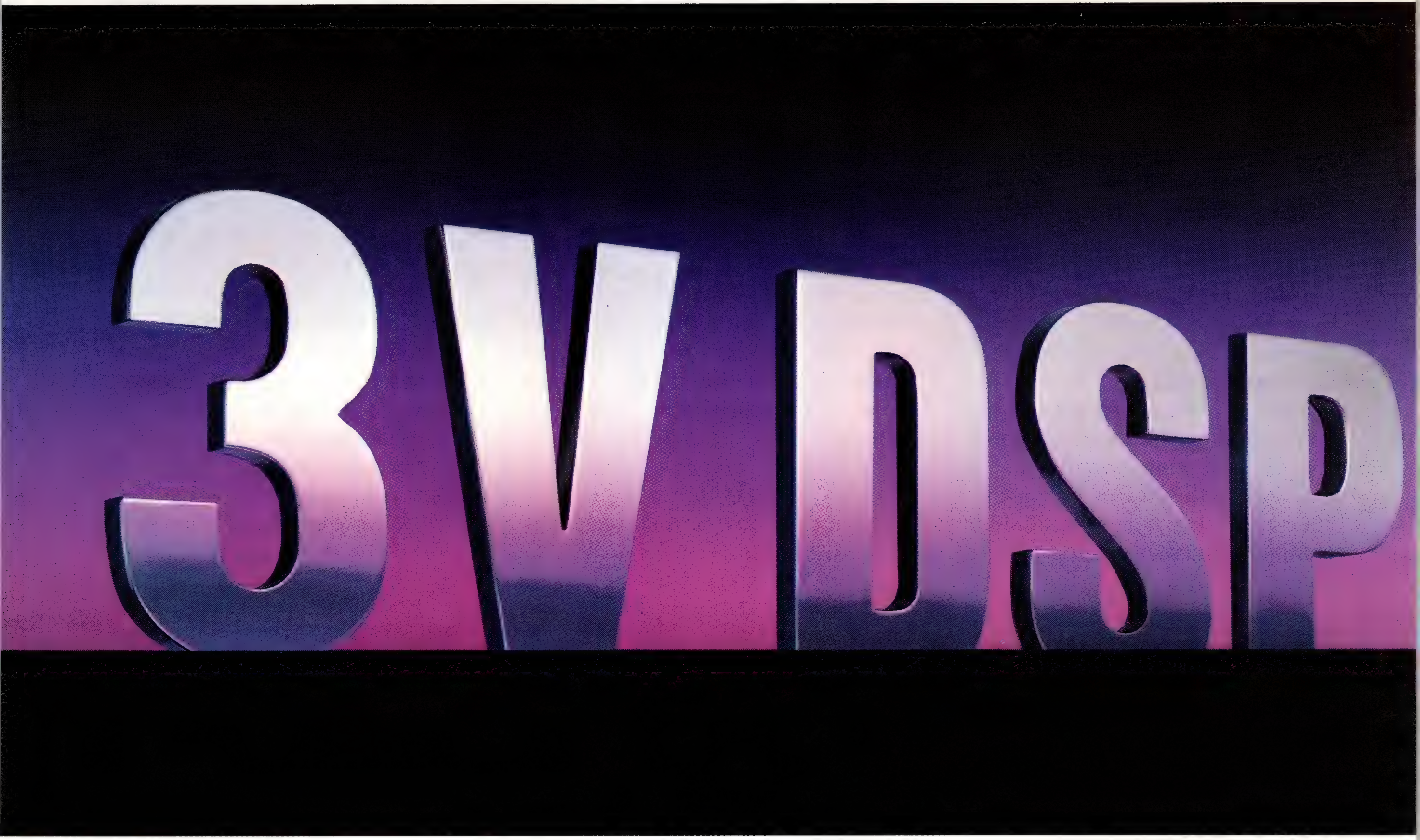

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back (for the test function), and switch-hook and ground-key detect outputs on separate pins. The HC-5506 SLIC meets CCITT and EIA transmission standards.

Any SLIC is a complex multifunctional device and the HC-5506 is no exception. As a result, only two of its unique circuits will be described: implementation of the ringing function and the "power sharing" technique, which permits linear control of over 2 W while dissipating less than 1 W. These circuits as well as the op amps that drive the telephone line are made possible by the move to bonded wafers *(Fig. 1, again)*.

## NO MORE RELAYS

When ringing a telephone, the SLIC must be switched off the line while the ring generator is switched on. In earlier SLICs, this function was implemented with a single-pole double-throw electromechanical relay. The telephone line is tied to the relay's pole pin, the ring generator to one "throw" pin, and the SLIC to the other "throw" pin. The resulting inherent break-before-make switching ensures that the SLIC and ring generator are *never* connected to the telephone line at the same time *(see the figure in "I thought BORSCHT was beet soup?," p. 63)*.

Bringing the ringing function on-chip requires the use of high-voltage semiconductor switches. A solid-state switch, be it a bipolar transistor, thyristor, MOSFET, or insulated-gate bipolar transistor (IGBT), lacks the near-zero on-resistance of a relay. Of all solid-state switch types, SCRs offer the lowest forward voltage drop per unit area of silicon (they're said to be "the most silicon-efficient"). However, SCRs conduct current in only one direction and their reverse breakdown voltage is lower than their forward breakdown voltage when they're off (not conducting). As a result, a pair of SCRs must be employed to form a single switch, one for each half cycle of the ringing waveform, and a reverse-blocking diode must be used in series with each SCR *(Fig. 1, lower left, exploded view.)*.

In such a circuit, the minimum forward voltage drop of an SCR runs about 1 V. This results in a dead zone around zero where neither SCR is conducting, which is a form of crossover distortion. The distortion isn't a problem for the ringing voltage with peaks as great as 150 V. However, a SLIC with voice signals of no more than a few volts creates such severe distortion, SCRs are rendered virtually unusable. Therefore, the HC-5506 switches the ringing voltage with SCRs but replaces them with gated amplifiers to switch the SLIC in and out of the circuit. That is, the SLIC-switching function is embedded in the transconductance amplifiers (G) that are used to drive the telephone line.

Removing the amplifiers' bias current forces their outputs into a high-impedance "tri-state" mode. During ringing and "wink off" (when the SLIC is disconnected from the telephone line), these amplifiers' high-impedance outputs remain connected to the telephone line. Here, the outputs are yanked around by the ringing voltage when it is switched in. No actual switch disconnects the SLIC from the line; instead, its internal current sources, differential pairs, resistors, and other devices that follow the output voltage, are rated at 250 V. The gated amplifiers eliminate any identifiable switching device that might cause crossover distortion between the telephone line and the SLIC.

These amplifiers also sense the ac (voice) Tip and Ring signal voltages across the 80-kΩ sense resistors

## I THOUGHT BORSCHT WAS BEET SOUP?

For years, the plain old telephone system, affectionately known as POTS, was a world unto itself with its own unique technology and language. However, over the past few years, it has taken full advantage of the semiconductor industry that it spawned over 45 years ago. In moving to solid-state switching (remember, the Bell Laboratories Nobel triumvirate that invented the transistor were looking for a better switch, not a linear device), the "BORSCHT" functions—Battery feed, Overvoltage, Ringing, Supervision, Coding, Hybrid, and Test—were put on line cards. Thus, the subscriber-line interface circuit (SLIC) and codec were born *(see the figure)*.

To reach other telephones, a telephone is connected to a switching exchange through miles of twisted-wire pairs. A home telephone (a subscriber) goes to a central office or exchange. The exchange also can be private (such as within a company), and in the past was called a private branch exchange, or PBX. Today, most PBXs have been replaced by a private-area branch exchange (PABX) full of line cards and digital switches.

The exchange contains the equipment required to run the telephone. When a call comes in, the exchange—using just the two telephone wires—must ring the telephone, detect when the telephone handset is picked up, stop the ringing, apply a dc voltage to the line to power the telephone, superimpose the incoming voice on the telephone line, and detect and transmit the audio from the telephone to the switching network. Though it performs other functions (like testing the line), the exchange's primary task is to switch the telephone line to other telephone lines. In the exchange, the circuits that actually drive the telephone line are called SLICs. The SLIC performs the previously mentioned BORSCHT functions, described here in detail:

*Battery feed:* The SLIC supplies the dc current required to power the telephone at the end of the twisted pair. Most telephones need at least 15 mA to operate. Because the line could stretch for many miles, it may represent a resistance of as much as 2000 Ω. Thus, the dc power supply for the telephone line—always a battery for reliability—is provided through the SLIC and must be on the order of 50 V (nominally 48 V).

*Overvoltage protection:* The long telephone line exists in an leading to the current mirrors. The currents from the mirrors are processed and applied as inputs to the transconductance amplifiers, which drive the telephone line. These currents represent a linear function of the telephone line's dc, ac, and longitudinal (common-mode) currents. The sense resistors remain in place when the ringing voltage is switched to the telephone line.

## CUT THE BIAS

The Ringing command from the codec filter cuts off the bias current to the amplifiers and turns on current sources connected to the SCR gates, thereby turning on the SCRs *(Fig. 1, again)*. While the "on" SCR passes the ring-generator voltage driving the telephone line from a low impedance, the "off" SCR is slightly reverse-biased and blocks it. When the ringing voltage crosses zero, both SCRs are briefly turned off. Then for the following half cycle, the "on" and "off" SCRs' functions are reversed in polarity. Because each SCR must be turned on again for each half cycle of the ringing voltage, the turn-on current sources are kept on during ringing. The collectors of the transistors forming the turn-on current sources also are exposed to the ringing voltage. As a result, they too must be rated at a potential of 250 V.

When a telephone is answered, the SLIC detects the "off-hook" condition and the turn-on current sources are removed. The "off" SCR remains off while the "on" SCR stays on. Rather than not being forced off, the SCR turns itself off at the beginning of the next half cycle when it becomes reverse-biased. The two SCRs forming the two switches, one at the telephone line's Tip wire and the other at its Ring wire, are now turned off. They remain off because the current sources are off.

During the time when the Ringing command is present, the SCRs must only be turned on when the ringing voltage is near zero. If either were turned on at ringing-voltage peaks, the instantaneous line-current steps might induce currents in other telephone lines creating noise.

Once the SLIC detects an an-

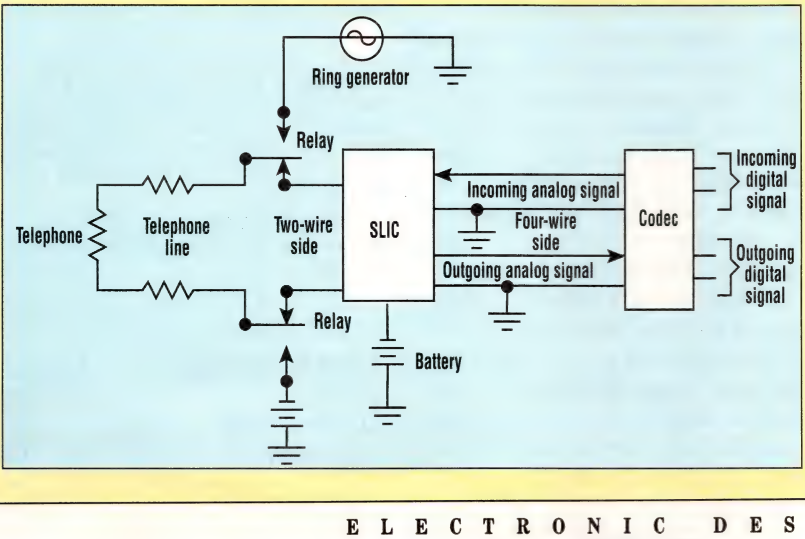
electrically "harsh" environments, such as getting hit by lightning or coming in contact with power lines. Even though lightning doesn't actually strike a telephone line, the lightning strike's millions of amperes of current can induce semiconductor-killing transients in a nearby line. The SLIC must protect itself—and the exchange—from any such transients on its line.

*Ringing:* The exchange contains a constantly running 93 V rms ac generator for ringing the telephone. When so ordered, the SLIC must switch the "hybrid" out of the telephone line and switch in the ring voltage.

*Supervision:* The SLIC must detect "service requests." These include detecting when the telephone is picked up to make or answer a call, and when it's hung up.

*Coding:* The outgoing signals from the SLIC must be digitized, and incoming digital signals from another SLIC must be converted to analog form.

*Hybrid:* The SLIC takes the incoming analog voice signal (or other audio signal, such as one from a modem) and superimposes it on the line on top of the dc current. Voice signals run on the order of 2 mA ac on top of the 15 mA of dc bias current. The SLIC also must detect the voice signal generated by the telephone and transmit it to the exchange to be sent on to another SLIC and its line. The incoming signal is on a separate line from the outgoing signal to allow digital conversion for transmission within and between exchanges. That's why this is referred to as the "Hybrid" function, because the incoming and outgoing signals are combined at the telephone-line connection to the SLIC. In other words, at a telephone, a speaker's voice (the one answering the telephone) and the incoming voice (the caller) are superimposed. This is called the two-wire side of the SLIC. At the exchange, the SLIC's input signal is separated from the outgoing signal and put on a separate pair of wires. This is called the four-wire side of the SLIC. Within an exchange, depending on its vintage, SLICs may be connected and switched via the four-wire analog lines or the codec I/O ports.



*Test:* The SLIC must switch test signals into the telephone line to detect faults on the line.

At present, no SLIC can perform all of the BORSCHT functions. Therefore, it's located on a pc board called a line card, which contains a codec and non-integratable components such as switching relays, large capacitors, and high-power clamp diodes to handle lightning strikes.

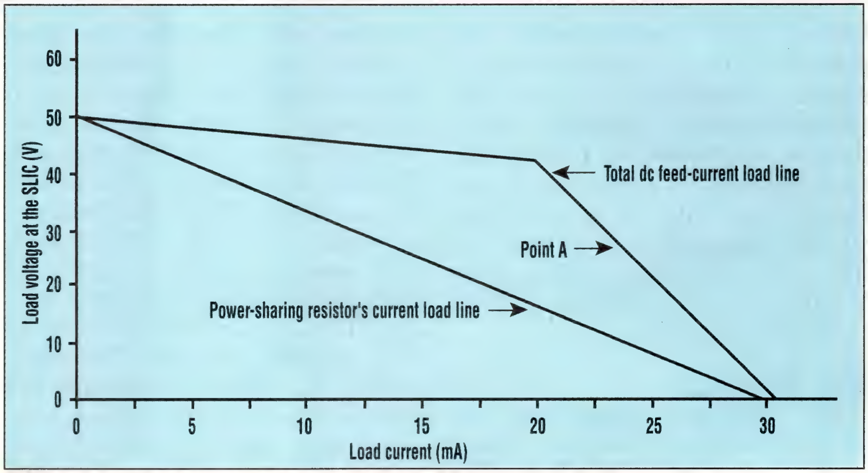
swered ringing phone (ring-trip detection), the amplifiers are kept in their tri-state mode until the SCR switches connected to the ring generator are off. However, as noted earlier, the SCRs don't turn off at the time the "off" command is given. One SCR will already be off and the other turns off when the next half cycle begins (when it becomes reverse-biased).

Thus, the circuit needs two zero-crossing detectors—one for current and one for voltage. When the Ringing command arrives, the zero voltage detector checks the ring generator output and only allows the SCRs to turn on when the ringing voltage is close to zero. When the SLIC detects a ring-trip condition, the zero current detector checks the telephone-line current. When the current is close enough to zero to ensure that the SCRs must be off, the detector informs the SLIC. It then supplies bias current for the amplifiers, turning them back on and connecting the SLIC to the telephone line.

## SYNTHETIC RESISTORS

As noted earlier, the combination of voltage and current controlled by a SLIC can easily result in dissipating power beyond the limit of most common IC packages. If conventional control techniques were used for the two-SLIC HC-5506, its 80-lead MQFP could not have handled the power. Consequently, the design team developed a pair of power-slashing techniques based on earlier work at Harris. First, the designers adjusted the "dc feed curve" to the telephone line. Telephone companies require the SLIC to deliver specified minimum dc currents at specified battery voltages and line resistances. As stated previously, meeting the requirements at the specified line loads leads to very high on-chip power levels at other unspecified but nevertheless real loads.

To beat the power-dissipation problem, the design team first synthesized an internal 200-Ω dc resistance on-chip for load currents below 20 mA. That is, for any telephone-line load drawing less than 20 mA, the SLIC (at dc) looks like a voltage source with 200 Ω in series with each line wire. If the line pulls more than 20 mA, the SLIC synthesizes a 2000-Ω source resistance. Put another way, if a load of 20 mA or less is placed between the SLIC's Tip and Ring pins, the SLIC looks like a 200-Ω resistor from Tip to ground and a 200-Ω resistance between Ring and battery. Every 1 mA of load current drops 400 mA across the SLIC—200 mV from ground to Tip and 200 mV from Ring to battery. In Figure 1, these resistors are shown in series with the output of the amplifiers.



**2. INTERNAL POWER DISSIPATION IS MINIMIZED** in the HC5506 dual SLIC. This is accomplished by sharing some of the telephone-line dc drive power with external power-sharing resistors. When there's 50 V across an open circuit line, no current flows through the SLIC or the resistors. When the line is shorted, the SLIC limits the load current to 30 mA, all of which flows through the power-sharing resistors.

## MINIMIZING POWER

At a load current of 20 mA, 8 V is dropped across the SLIC (the sum of 200 Ω plus 200 Ω multiplied by 20 mA). As a result, each additional milliampere over 20 mA creates a change of 4 V across the telephone line. This synthesized double-mode impedance includes the specified operating points while minimizing SLIC power, particularly when used with off-chip power-sharing resistors. These resistors, connected to the Tip and Ring terminals, are enclosed within the transconductance-amplifier's local feedback loop and share the task of driving the telephone line. The amplifier controls the line current but delivers only a portion of it to the line, while the external power-sharing resistors deliver the rest. Depending on the telephone-line length, the line can look like a load that varies from 200 to 2000 Ω. The local feedback loop adjusts the percentage of current between the amplifier and the power-sharing resistors, depending on the load presented to the SLIC, to keep its power below about 250 mW/SLIC for all conditions.

In this circuit, for a given load, the SLIC's dc feedback sets the load voltage and current according to the "total dc-feed" load line *(Fig. 2, again)*. Under these load conditions, the power-sharing resistors deliver the portion of the load current determined by the power-sharing resistors' load line. The SLIC now delivers the difference current between the pair of load lines. For example, at the load conditions indicated by point A, the SLIC sets the load at 22.5 mA and 31.5 V. At a voltage of 31.5 V, the power-sharing resistors deliver a current of 11 mA and the SLIC delivers 11.5 mA.☐

### PRICE AND AVAILABILITY

*The HC-5506 dual solid-state SLIC in its 80-pin MQFP goes for $15 each in quantities of 100, or just $7.50 per telephone line. Small quantities will be available within 30 to 60 days.*

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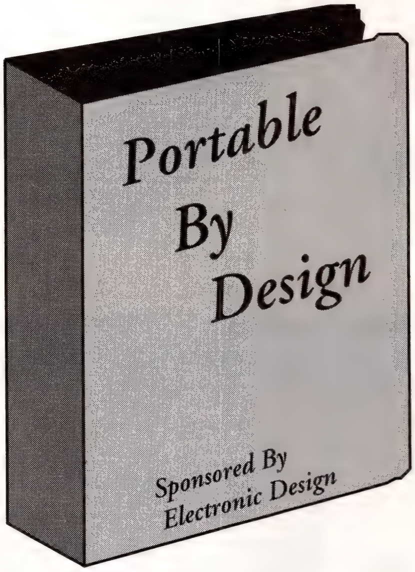

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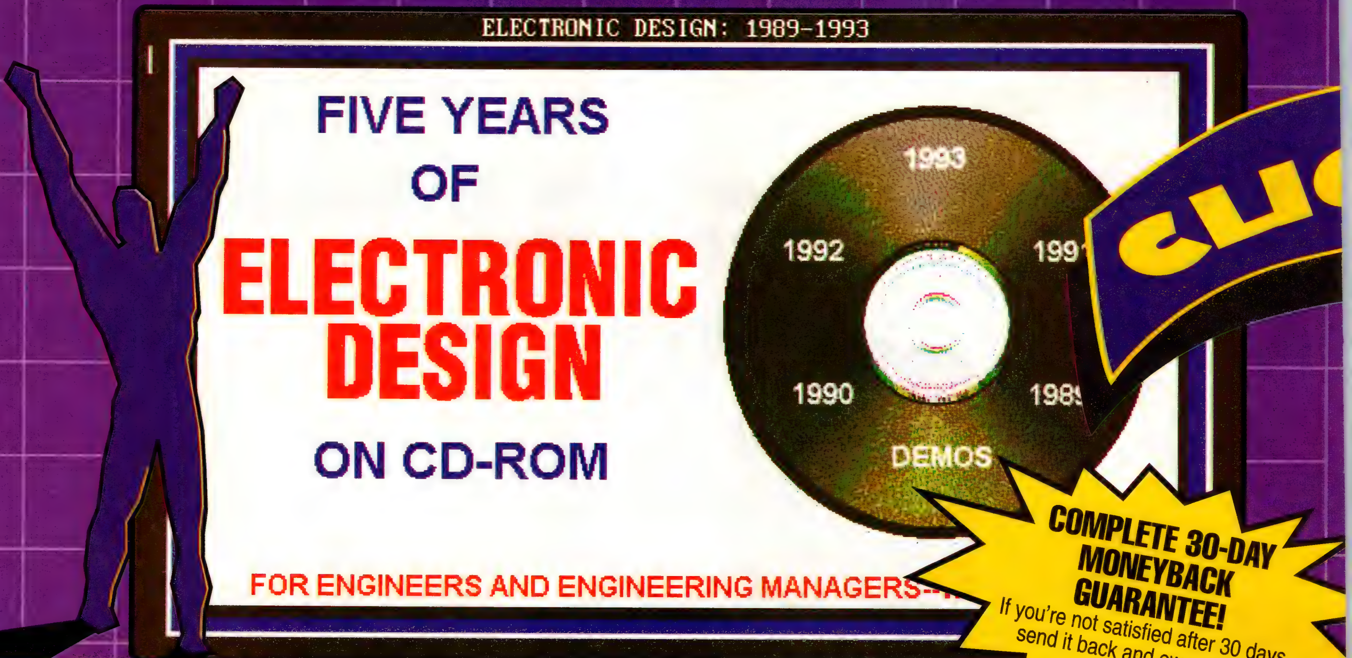

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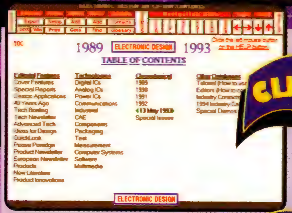
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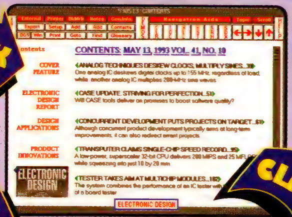
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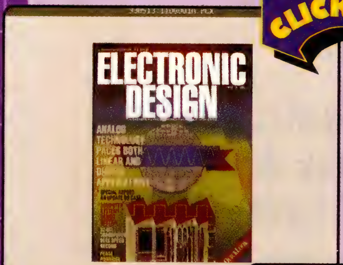

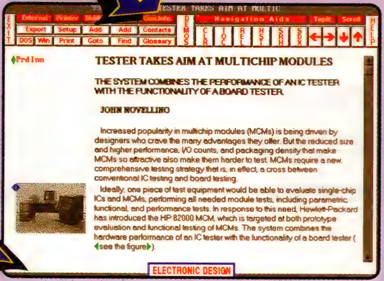
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TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is being driven by designers who crave the many advantages they offer. But the reduced size and higher performance, I/O counts, and packaging density that make MCMs so attractive also make them harder to test. MCMs require a new, comprehensive testing strategy that is, in effect, a cross between conventional IC testing and board testing.

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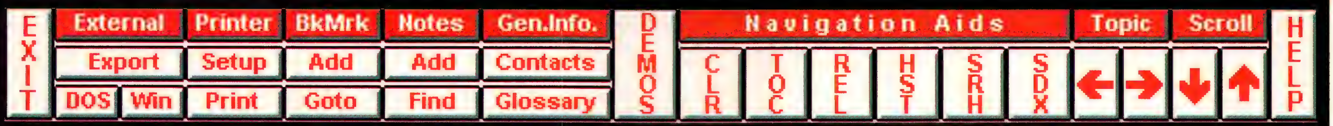

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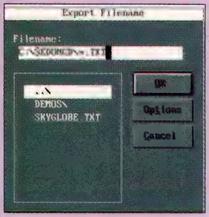

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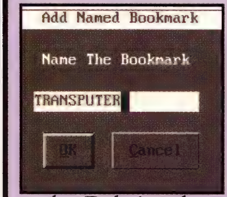
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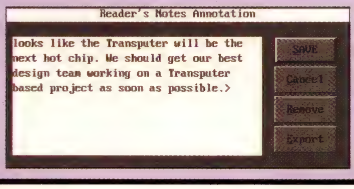
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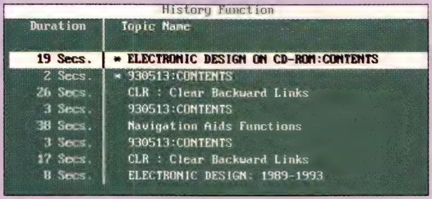
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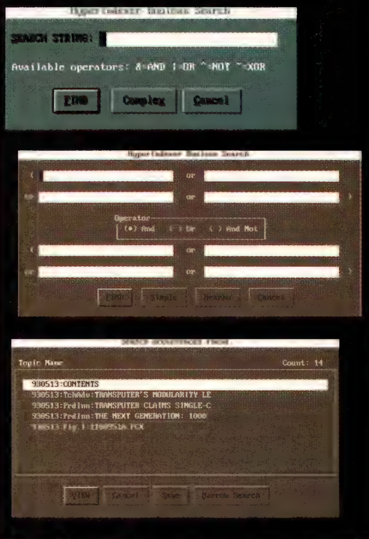
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Topic Name                         Count: 14

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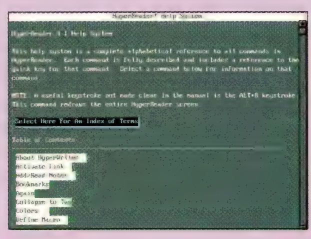
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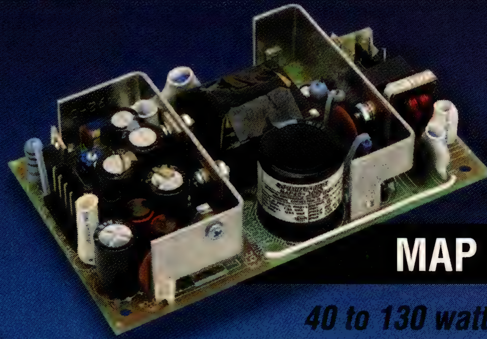

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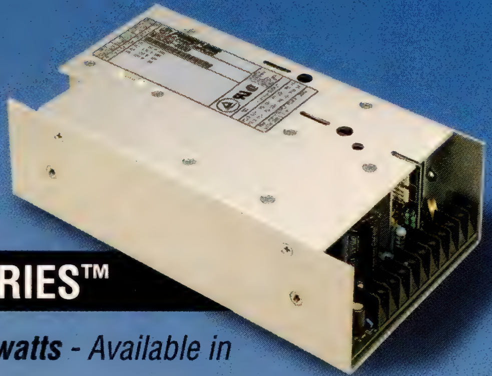

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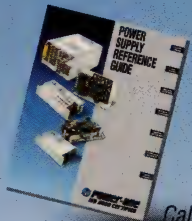

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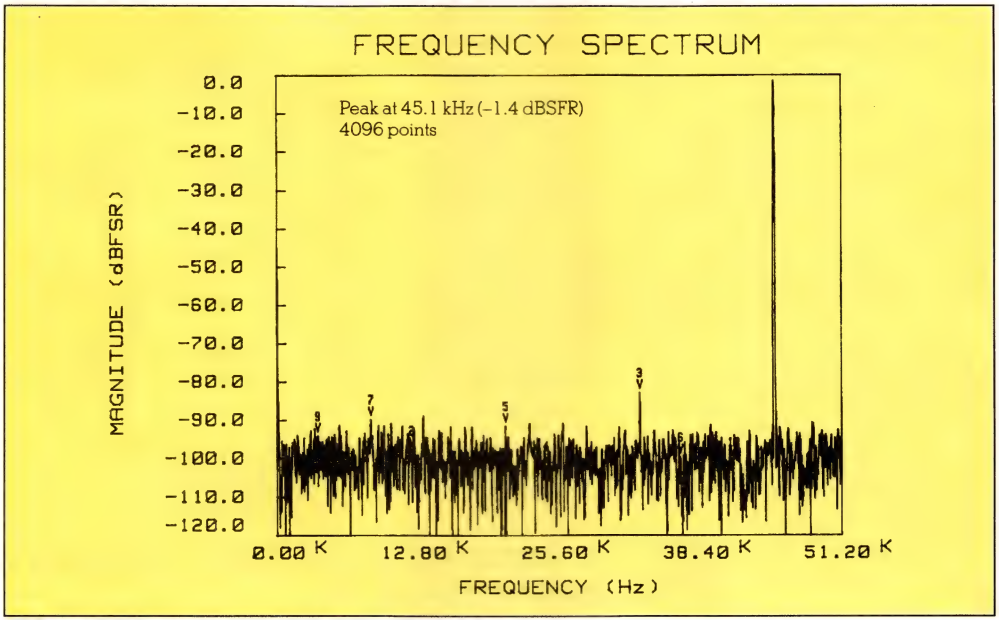


**1. THIS FREQUENCY SPECTRUM** shows the FFT results from the 102.4-kHz digitization of an analog input signal. The signal is the sum of a 45.1-kHz sine wave and a 147.5-kHz sine wave.

## DESPITE WHAT MANY BELIEVE ABOUT THE NYQUIST THEOREM, UNDERSAMPLING IS DESIRABLE IN CERTAIN APPLICATIONS.

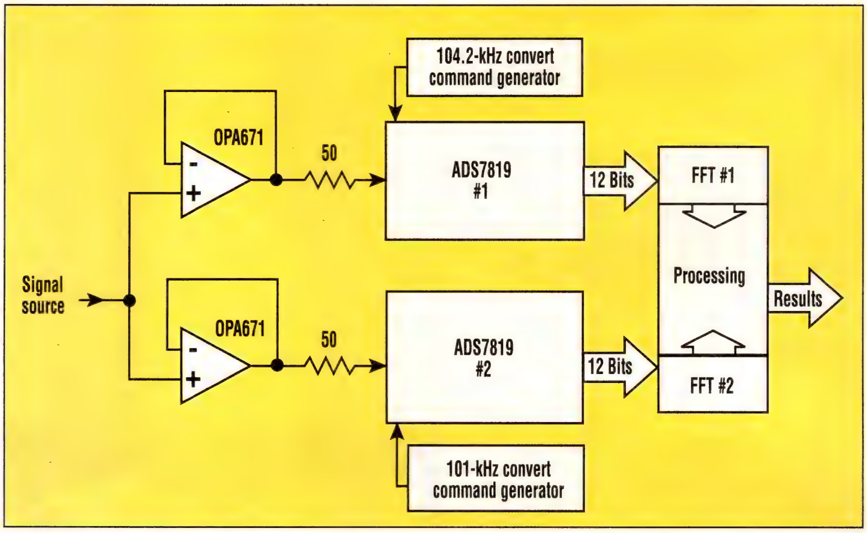
# THE BENEFITS OF UNDERSAMPLING

The past decade has seen tremendous improvements in both the hardware and software needed to do extensive digital signal processing (DSP). On top of that, there's been an increase in the number of sampling analog-to-digital converters (ADCs) that can accurately capture dynamic signals. Applications involving DSP span from digitizing audio signals in consumer products to vibration analysis in industrial markets to a whole range of uses in wireless- and satellite-communications systems.

Unfortunately, though, much of the literature published during this period concerning acquisition and digitization of real-world signals has been misleading or incorrect. This has been particularly apparent in many of the discussions concerning Nyquist, and the supposed limitations that his theorem places on sampling rates.

This article will present an application idea for using undersampling in a way that

**GEORGE HILL**
Burr-Brown Corp., M/S 122, P.O. Box 11400, Tucson, AZ 85734; (602) 746-7283.



**2. THE SIMPLE BLOCK DIAGRAM** of a dual-rate sampling system shows how a signal is sampled, converted, and processed.

clarifies much of the confusion about what the Nyquist theorem says, as opposed to what many have misinterpreted it to mean. In particular, an output spectrum *(Fig. 1)* will be shown to contain two different input frequencies (45.1 kHz and 147.5 kHz), and undersampling will be used to determine this. However, before getting into the application, it makes sense to discuss DSP trends that support signal analysis. It's also a good idea to review why the Nyquist theorem really doesn't limit usable bandwidth to input signals that are dc to half of the sampling frequency, as is often assumed. Finally, the article will discuss reasons why undersampling may be desirable in real-world applications.

## DSP TRENDS

Digital-processing speed continues to increase rapidly as costs spiral further downward. One of the fast-growing digital-IC niches riding this trend over the past decade has been chips dedicated to DSP applications. More recently, this DSP power has become accessible to an ever-growing community of designers, with both software and hardware development tools emerging.

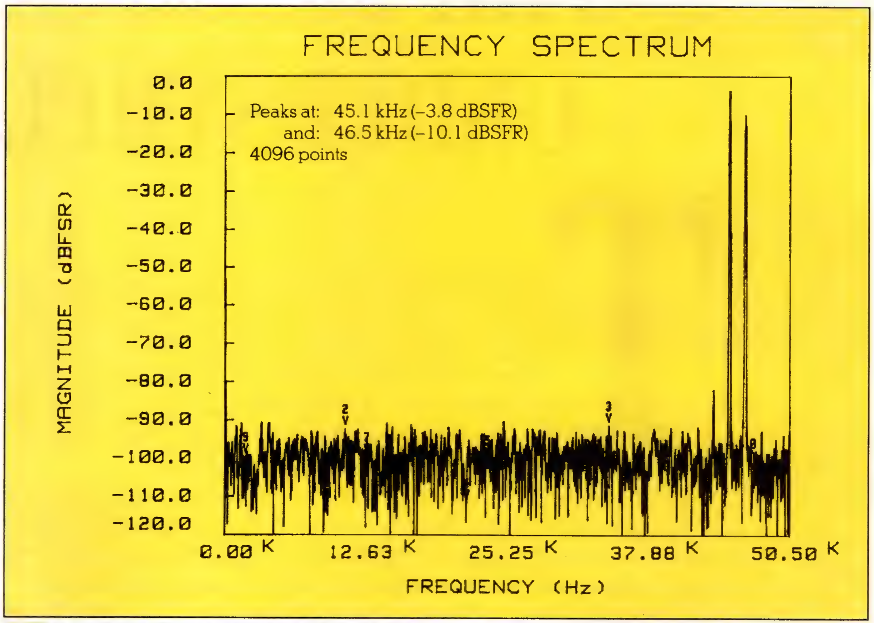
Over the same period, suppliers of ADCs have increasingly included sample-and-hold circuits on new ADCs, and tested and specified these converters with dynamic input signals. Like digital ICs, ADCs have seen significant performance and speed advances while prices have declined.

The enhanced yet less expensive digital and analog ICs needed to implement DSP for real-world systems has opened up a large number of application areas. Another way to look at this would be to say that the performance needs for these applications were the market drivers for the development of the DSP and ADC ICs.

Cellular phone systems (which include both the phones themselves and the base stations) and PC-based multimedia systems are the DSP applications most visible to the general public today. However, DSP is rapidly finding its way into areas like vibration analysis for industrial equipment, electronic automobile mufflers, and power-factor monitoring, which is becoming crucial due to the PCs and wireless phones that are connected asynchronously to power mains.

In many discussions concerning Nyquist criterion, it's assumed that the input signal must be limited before going into the ADC. However, that assumption isn't derived from the theorem itself. It is true that it's impossible to know from one set of digitized data alone what frequencies were in the original signal (subsequent discussion and equations will illustrate why this is true). Thus, it's understandable when many designers, and authors, jump to the conclusion that the input to the ADC must be limited so that it contains no frequencies above $f_S/2$.

Good engineers know that a single set of digitized data limits subsequent analysis to an $f_S/2$ bandwidth, unless there is additional information. Consequently, without even thinking about it, they construct a source for that additional information. The extra information usually takes the form of an antialiasing filter in front of the ADC, which limits the input-frequency bandwidth that the ADC sees, and thus limits what frequencies can



**3. IF THE SAMPLING RATE** from the first FFT is changed from 102.4 kHz to 101 kHz, the 45.1-kHz input still appears in the 45.1-kHz bin, while the 147.5-kHz signal aliases back into the 46.5-kHz bin.

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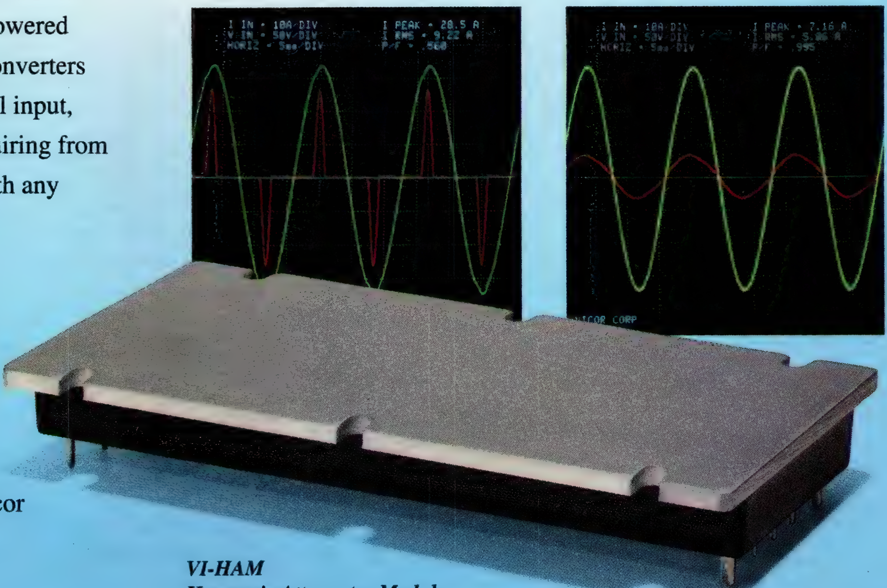

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be present in the digitized data. Still, the Nyquist theorem itself imposes no such limitation.

The Nyquist theorem does place limitations on the information that can be derived from digitized data. Basically, after collecting a data set of n points at a sampling rate of fs, all of the original signal's information is confined to an fs/2 bandwidth broken down into n/2 frequency bins.

For example, without additional information about the original input signal, it's impossible to look at the plot of a fast-Fourier-transform analysis and determine whether any specific bin contained energy from a particular frequency between dc and light. The FFT results will show how much energy was included in a specific fs/n section of the fs/2 bandwidth. However, each of the fs/n sections can contain an infinite number of frequency components distributed at fs/2 intervals from dc to light.

In Figure 1, there's no way to determine from the single set of digitized data alone that the actual input spectrum resulted from a 45.1-kHz signal summed with a 147.5-kHz signal. The data also could have resulted from a single tone at 10.2851 MHz, several tones within a few hertz of 45.1 kHz, or any of an infinite combination of input frequencies. The data clearly shows that there's no significant input signal in the other frequency bins (which cover an even larger number of possible frequencies in the original spectrum), but that doesn't help.

The real world imposes limitations relative to sampling signals and maximizing the information contained in a digitized data set. If there's any jitter in the system, this will increase the noise in the digitized data. The main sources of jitter are located in the sampling switch of the ADC, and in the system circuitry that generates the convert command. When testing a system in the lab, jitter also may be injected by the signal generator driving the ADC. Similarly, because signal-conditioning circuitry and the sample-and-hold amplifier used in front of the ADC have finite bandwidth in all real-world applications, they will contribute distortion to the digitized data. This distortion increases with input frequency. Jitter and distortion are the primary limitations on the bandwidth capability of any digitizing system, but the relative contributions from various sources is difficult to predict or analyze at higher frequencies.

## WHY UNDERSAMPLE?

It may be easier to relate to an application using undersampling if we first review some practical reasons for using this strategy. One common motivation for considering undersampling is the desire to reduce the speed requirements on the digital section of the system. Consider an analog signal of interest with a bandwidth of 50 kHz, centered on 4.975 MHz. Without using undersampling, an analog-to-digital conversion rate of at least 10 MHz would be required, and the digital side of the system would need to be able to capture the data at this rate. However, the Nyquist theorem only

## AN ALTERNATIVE TO ANALOG ANTIALIASING

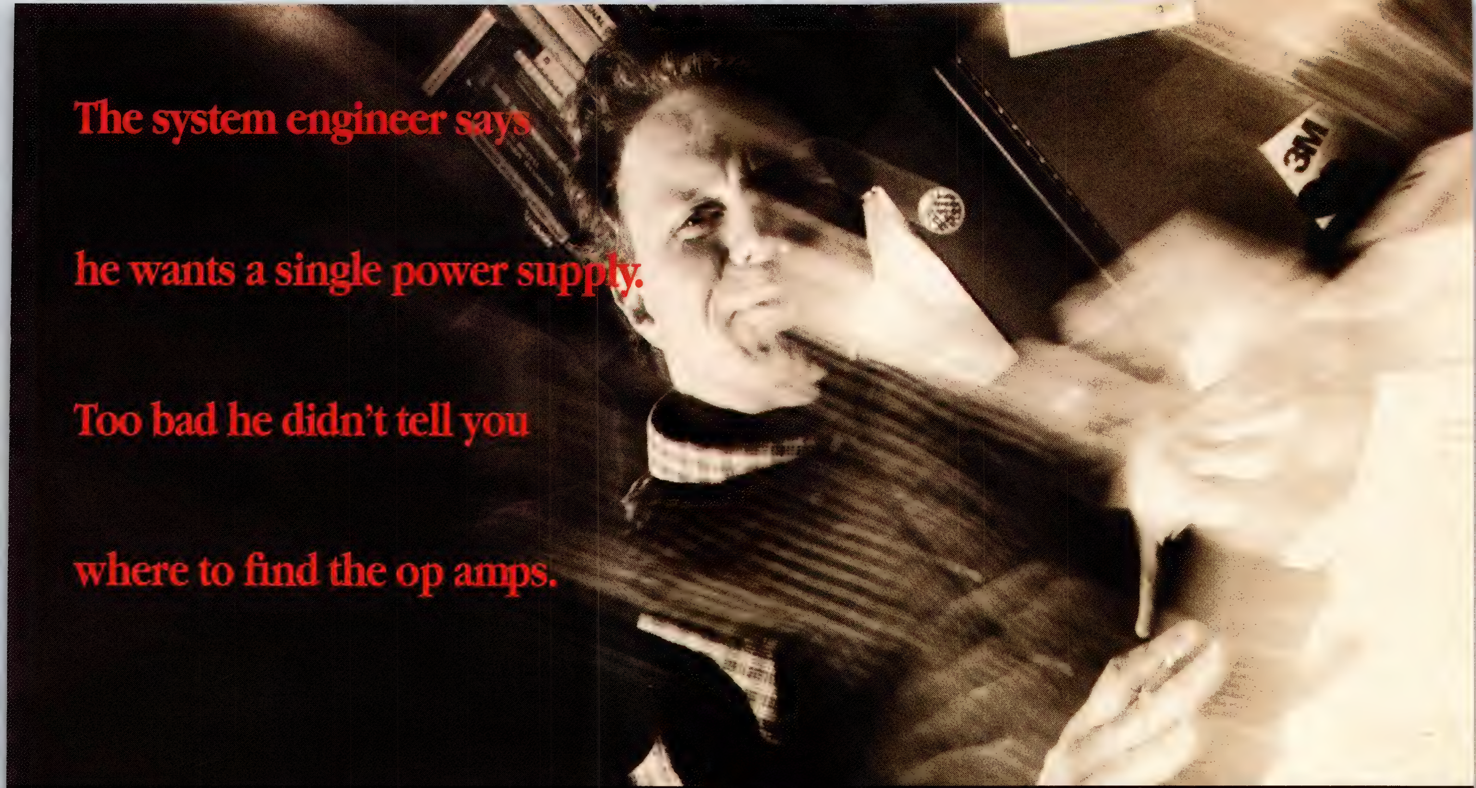
One reason that I wrote this article was to come up with a response to some of my internal critics concerning specifications on Burr-Brown's recently introduced ADS Family of 12- and 16-bit analog-to-digital converters. These sampling ADCs have performance tested and guaranteed for input frequencies much closer to fs/2 than has been normal in the past. Such results can raise questions (ask my test engineers!) about the usefulness of these specifications in real-world applications.

For example, the 100-kHz sampling rate, 16-bit ADS7805 is guaranteed to have total harmonic distortion no worse than –90 dB (for the low grade part) with a 45-kHz input. The main question from my critics is whether this specification has any value in real applications, because the cost and complexity of an analog antialiasing filter to roll off 90 dB between 45 and 55 kHz is prohibitive. Our ADC costs only about $30, compared to an off-the-shelf brick-wall filter that can easily go for five times as much. And it still requires careful analysis of the filter's ripple and phase characteristics.

The application discussed in the main article, which uses two ADCs with different sampling frequencies, may offer a reasonable alternative to expensive analog antialiasing filtering in some applications. In Figure 1, the output spectrum is shown for an input that was the sum of a 45.1-kHz sine wave and a 147.5-kHz sine wave, sampled at 102.4 kHz. The second sampling ADC, with the output spectrum in Figure 2 illustrates that the input signal actually contained two different frequencies. The two sets of data make it possible to identify the original input frequencies and their amplitudes.

Digital signal processing could be applied to these two sets of data to remove (filter out) the effects of either of the original input signals. The cost will be increased processing time, software, and computing power, but this higher cost already may be less than the cost of analog filtering, and will most likely decrease further as digital trends continue. Also, this approach could allow for a software-selectable bandwidth, which isn't a reasonable option with analog filtering. This holds especially true if the application requires more than about 10 bits of accuracy, because of real-world limitations on cost-effective programmable analog filters.

The main reason for specifying the new ADS Family for performance near fs/2 is the simple fact that we do not want the ADC to limit the performance of most real circuits. Typically, an ADC that samples at 100 kHz will have specifications based on an input frequency of 1 kHz. Therefore, designers with applications for higher input frequencies must estimate expected performance based on typical performance curves in the data sheets. With performance guaranteed for a 45-kHz input, users can be highly confident that in-system performance will be as good or better at any lower input frequency.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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
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| OP | 113 | 213 | 413 | | • | • | • | | | 75 | 4.7 | ±40 | 1.75 | 3.4 | Lowest noise and drift |
| OP | 183 | 283 | | • | • | • | • | | | 1000 | 10 | ±25 | 1.5 | 5 | 5 MHz from +3 to +36V |
| OP | 90 | 290 | 490 | 1.6 | • | • | • | | | 150 | 60 | +13/-7 | 0.015 | 0.02 | Precision micro power |
| OP | | 291 | 491 | • | • | • | | • | • | 700 | 21 | ±10 | 0.35 | 3 | Low power R-R I/O |
| OP | | 292 | 492 | | • | • | • | | | 800 | 15 | ±8 | 1.4 | 4.5 | Low cost |
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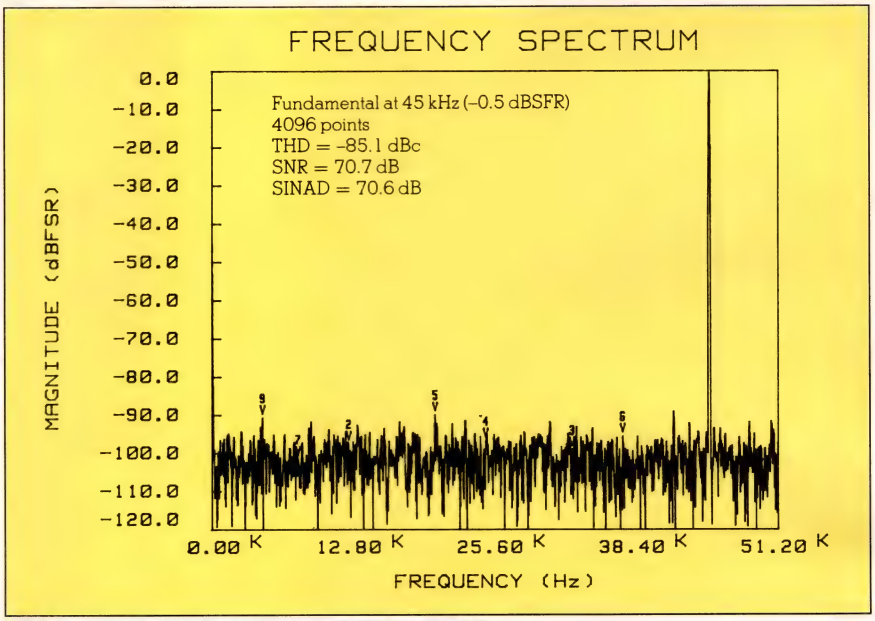


**4. THIS FREQUENCY SPECTRUM** illustrates a 45-kHz input sampled at 102.4 kHz. The fundamental shows up in the 45-kHz bin.

requires a sampling rate of 100 kHz (assuming no other frequencies alias into the output of the ADC) to get all useful information out of the input signal. This means that slower digital circuitry could be used, or other tasks can be interleaved with the collecting of the digitized data from the ADC.

In the above example, power and money also can be saved in the ADC section of the circuit. The sample-and-hold amplifier needs to have the same capabilities for both conversion rates, but a 100-kHz ADC tends to be smaller, use much less power, and cost significantly less than a 10-MHz ADC with the same resolution.

Undersampling also may be a viable way to extend the capability of existing systems with relatively minor redesign rather than starting from ground zero. No circuit redesign is needed beyond possibly having to increase the bandwidth of the analog-signal-conditioning circuitry up to and including the sample-and-hold amplifier, as long as there's a method (such as the one described below) to identify what input frequencies are reaching the ADC input.

Yet another use for undersampling is eliminating a complex analog antialiasing filter *(see "An alternative to analog antialiasing," p. 72).*

## EXTENDED BANDWIDTH

Figure 1 illustrates the FFT results from digitizing at a 102.4-kHz rate an analog input signal that's the sum of a 45.1-kHz sine wave and a 147.5-kHz sine wave. Traditionally, one way to determine the amplitudes and frequencies in an arbitrary input signal would be to collect multiple sets of data and perform separate FFTs. The analog filter in front of the ADC needs to change to limit the inputs at the ADC to manageable bandwidth segments less than $f_S/2$ wide. Another approach would be to simultaneously digitize the input signal at two slightly different sampling rates, and use the two sets of output data to determine the original input spectrum.

When implementing a dual-rate sampling system *(Fig. 2)*, it's useful to review how an input sine wave $f_{in}$ will show up in an FFT analysis of a set of data taken at an $f_S$ sampling rate. For any $f_S$, the following equation calculates the frequency bin b in an FFT that measures the energy of a sine wave of frequency $f_{in}$ in the original input signal:

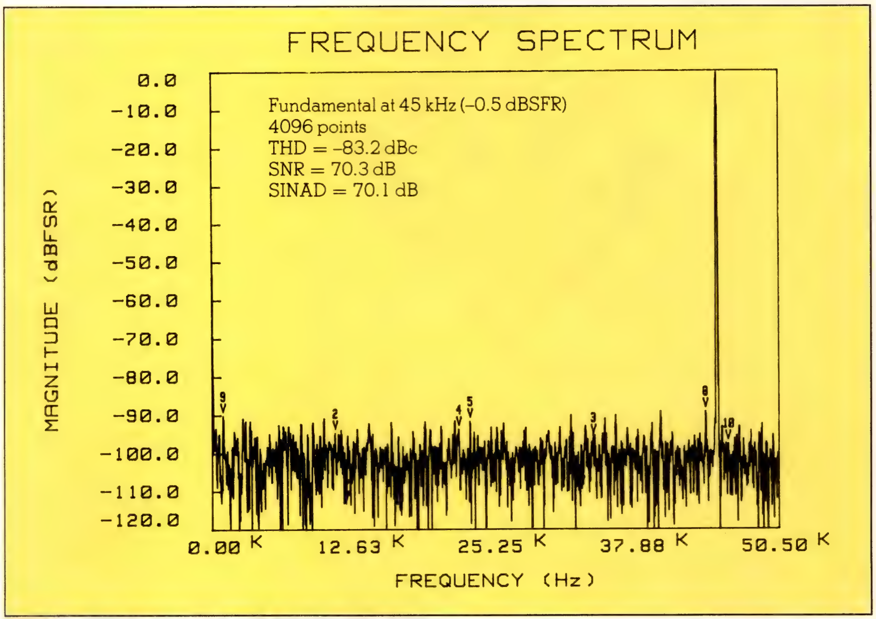
$$b = (-1)^i \left[ f_{in} - \left( i + \frac{1-(-1)^i}{2} \right) \frac{f_s}{2} \right] \qquad (1)$$

where:

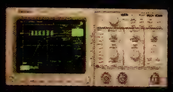
$$i = \text{Largest integer} \le \frac{2f_{in}}{f_s} \qquad (2)$$

To further explain, i is the number of times the spectrum is folded back. With a 102.4-kHz sampling rate, an input signal of 45.1 kHz (i = 0) will show up in the 45.1-kHz bin, as will a 147.5-kHz input (i = 2). If the sampling rate were changed to 101 kHz, the 45.1-kHz input still shows up in the 45.1-kHz bin, while the 147.5-kHz signal aliases back into the 46.5-kHz bin *(Fig. 3)*.

For this dual-sampling technique to be of use, the frequency of an arbitrary input signal must be identifiable. Equation 1 works when the in-



**5. THE SAME 45-KHZ INPUT** from Figure 4 is now sampled at 101 kHz. The fundamental still appears in the 45-kHz bin.



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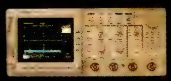

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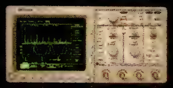

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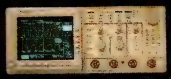

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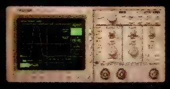

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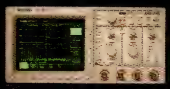

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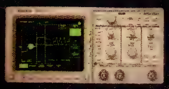

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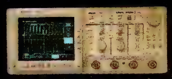

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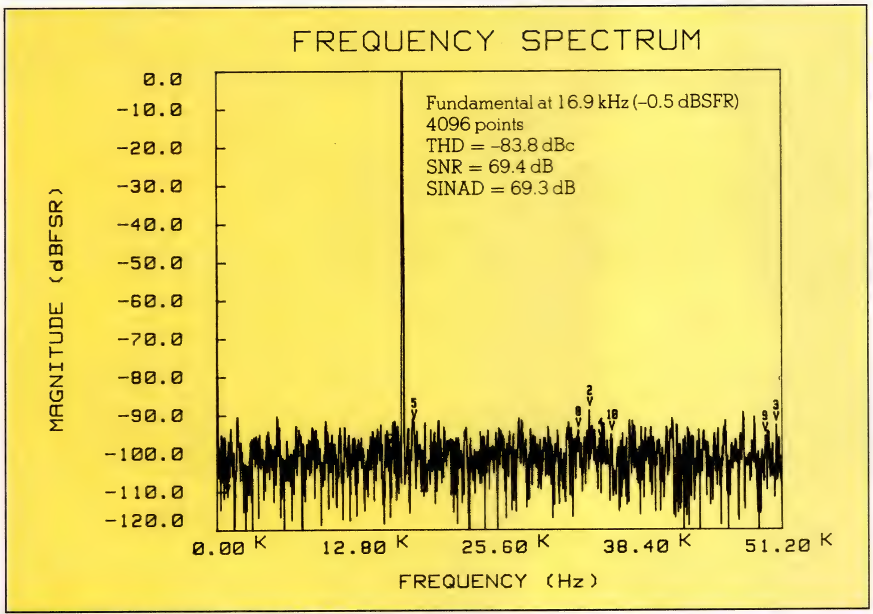


**6. THIS PLOT REVEALS** that a 495.1-kHz input sampled at 102.4 kHz has its fundamental in the 16.9-kHz bin.

put frequency is known, but needs to be modified to identify the original input-signal frequency components from two sets of digitized data. As previously discussed, the presence of a peak in bin b of an FFT analysis can result from an infinite number of different input frequencies. These frequencies are at discrete intervals related to $f_S$ as follows:

$$f_{in} = (-1)^i b + \left( i + \frac{1-(-1)^i}{2} \right) \frac{f_s}{2} \qquad (3)$$

$$i = 0,1,2,3,\ldots$$

In equation 3, i can theoretically take on any integer value from 0 to infinity. Thus, the presence of a peak in bin b doesn't clearly identify the actual input frequency. Using a dual-rate sampling technique can help this situation significantly. Solving Equation 3 for two different rates ($f_{S1}$ and $f_{S2}$) and the frequency bin of interest in each ($b_1$ and $b_2$) will result in:

$$f_{in1} = (-1)^n b_1 + \left( n + \frac{1-(-1)^n}{2} \right) \frac{f_{s1}}{2} \qquad (4)$$

$$n = 0,1,2,3,\ldots$$

$$f_{in2} = (-1)^m b_2 + \left( m + \frac{1-(-1)^m}{2} \right) \frac{f_{s2}}{2} \qquad (5)$$

$$m = 0,1,2,3,\ldots$$

Finding values of n and m where $f_{in1} = f_{in2}$ will determine actual input frequencies that could generate the peaks in the FFT bins. In the empirical tests that will be described shortly, frequencies above 2 MHz were uniquely identified. Because the distortion starts to increase significantly on the ADC at that frequency, higher input frequencies weren't tested.

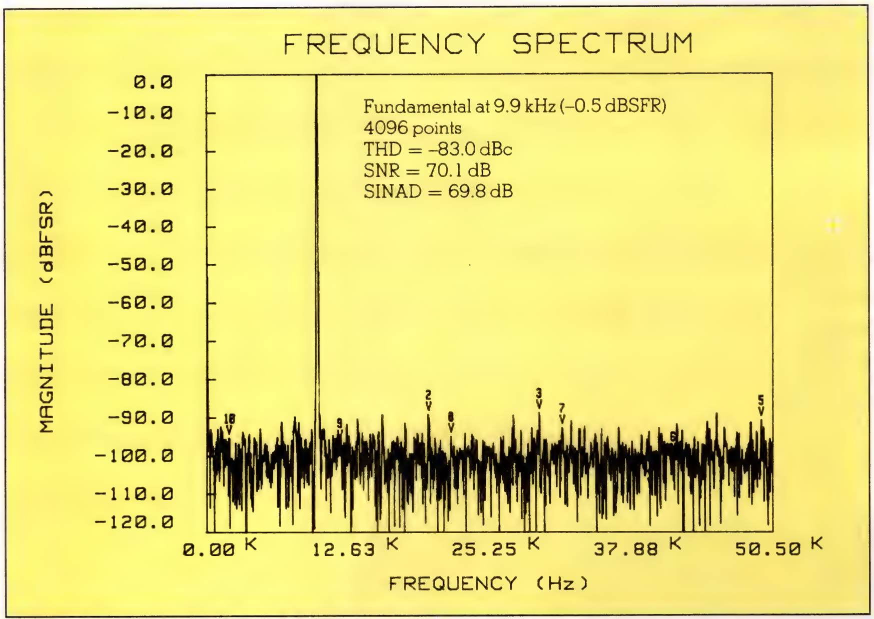
Calculating the frequencies at which the FFTs start repeating the pattern of lower-frequency input signals is encouraged. In other words, it's beneficial to determine the spacing of the n and m values that start repeating solutions to $f_{in1} = f_{in2}$, because n and m can go to infinity. As a hint, the FFT results seen for all frequencies between dc and $f_S/2$ are first repeated for inputs somewhere above 50 MHz when implementing the dual-rate technique using 101- and 102.4-kHz sampling rates.

## PRACTICAL APPLICATIONS

In practical applications, the math starts to get fairly complicated. This is partly due to the fact that the number of data points (samples) in each FFT must be factored in, because it affects the bin width in the FFTs. What this repetition means for practical applications is that some form of antialiasing filtering in front of the ADC may be required to implement a dual-rate approach. In some applications, the bandwidth limitations of the input-signal-conditioning circuitry and the ADC may provide enough inherent filtering of higher input frequencies; in other cases, a simple passive RC filter is all that's needed.

Another set of constraints at specific lower frequencies also falls out of solving for $f_{in1} = f_{in2}$, and will require consideration before implementing this approach in some applications. Assuming $f_{S2} > f_{S1}$, then any input signal at frequency:

$$p\left( \frac{f_{s2} - f_{s1}}{2} \right) \qquad (6)$$



**7. WHEN THAT SAME** 495.1-kHz input from Figure 6 is sampled at 101 kHz, the fundamental appears in the 9.9-kHz frequency bin.

will be indistinguishable from an input signal at:

$$p\left(\frac{f_{s1}+f_{s2}}{2}\right) \qquad (7)$$

and any input signal at:

$$\frac{f_{s1}}{2} - p\left(\frac{f_{s2}-f_{s1}}{2}\right) \qquad (8)$$

will be indistinguishable from an input signal at:

$$\frac{f_{s1}}{2} + p\left(\frac{f_{s1}+f_{s2}}{2}\right) \qquad (9)$$

where p can be any integer starting at 1. There are no conflicts at any other frequencies, until the input signal reaches the very high frequencies where the whole spectrum starts repeating. These potential problem frequencies should be tolerable in many applications for several reasons: they are predictable, don't start until above the lower sampling frequency, occur relatively seldom, and can be placed where desired by choosing appropriate sampling frequencies.

The Burr-Brown ADS7819 was used to test the dual-rate sampling system described previously *(Fig. 2, again)*. This is a 12-bit sampling ADC, which is specified for conversion rates up to 800 kHz, was chosen because the input sample-and-hold is accurate well beyond its 400-kHz fs/2 rate. In fact, this ADC maintains excellent performance digitizing 1.5-MHz full-scale inputs, with SINAD still at 60 dB, or roughly 10 bits.

## SPREADSHEETS

With due apologies to Bob Pease, a spreadsheet was used to determine original input frequencies from data sets digitized at 102.4 kHz and 101 kHz. Pease is correct when he says that spreadsheets can lead to gross errors if misused to replace thinking and common sense. They can be an excellent tool to test theories and assumptions, and to implement repetitive tasks, as was done to solve Equations 4 and 5. Using a spreadsheet to attempt to implement the derived equations also eased the task of finding errors in the original derivations—about half the problems that were found related to the derivation, while the other half were with the spreadsheet. Neither alone would have yielded the final results as quickly, at least for the author, who hasn't attended college math classes for quite some time!

In developing this article, a number of pairs of data sets were taken using a dual-rate ADS7819 sampling system for various input frequencies from dc to above 1 MHz. These pairs of data sets were then independently analyzed to see how well the original input frequency could be determined from the digitized data alone. Each of the actual input sine-wave frequencies was accurately determined using Equations 6 through 9. Reviewing the results for several of the input frequencies shows empirically how the dual-rate approach works *(Figs. 4 through 9)*.

Figures 4 and 5 show results from one of the sets of data. In both of these FFTs, the fundamental shows up in the 45-kHz bin. Using Equations 4 and 5, we can calculate that this means the input frequency actually was 45 kHz. This is just what we should intuitively expect, because the dual-rate technique detects aliasing by the shift in fundamentals in FFTs calculated from data taken at different sample rates.

Figures 6 and 7 show that the fun-

## HOW TO DETERMINE THE PROPER UNDERSAMPLING RATE

After a recent applications seminar given by Burr-Brown in Rome, Italy, one of the attendees suggested an approach for easily calculating appropriate sampling rates for undersampling any specified range of input frequencies. He offered his ideas for inclusion in future seminars, but didn't authorize us to use his name. Here is his approach (but give me credit for any errors or misunderstandings because his original was longer):

Assume that the bandwidth of interest to be digitized ranges from a lowest frequency of interest ($f_L$) to the highest frequency ($f_H$). For the full range of $f_L$ to $f_H$ to be unambiguously represented after digitization at a sampling rate of $f_S$, the following two equations must hold:

$$\frac{kf_s}{2} < f_L \qquad (A)$$

$$f_H < \frac{(k+1)f_s}{2} \qquad (B)$$

where k = 0, 1, 2, 3, 4, etc. (any integer). Meeting these two conditions simply divides $f_S$ into discrete segments, where $f_L$ is fast enough to be more than k/2 times $f_S$, and $f_H$ is slow enough to be less than (k + 1)/2 times $f_S$. Solving for $f_S$ yields the equation:

$$\frac{2f_H}{k+1} < f_S < \frac{2f_L}{k} \qquad (C)$$

which is the interval of allowed sampling frequencies. Removing $f_S$ from Equation 3 yields:

$$\frac{2f_H}{k+1} < \frac{2f_L}{k} \qquad (D)$$

which can be used to define the maximum allowable value of k as follows:

$$k < \frac{f_L}{f_H - f_L} \qquad (E)$$

The highest value of k that meets the conditions of Equation E determines the maximum undersampling that will keep the full $f_L$-to-$f_H$ bandwidth in the digitized output.

Furthermore, the parity of k determines whether the order of the spectral bins in an FFT analysis is preserved or inverted. In other words, if k is even, then $f_H$ will show up in a spectral bin to the right of $f_L$ (which is obviously the case when k = 0 and no undersampling is done), and $f_H$ will show up in a spectral bin to the left of $f_L$ when k is odd.

Let's look at an example: if we want to digitize a 50-kHz bandwidth signal riding on a 1-MHz carrier, then $f_L$ = 975 kHz and $f_H$ = 1025 kHz. Solving Equation E shows us that k can be no greater than 19. Because k = 19 would yield an inversion in the spectral location of the $f_L$ and $f_H$ bins after digitizing, let's choose k = 18, and solve Equation C for an acceptable fs range:

$$107.9\text{ kHz} < f_s < 108.3\text{ kHz} \qquad (F)$$

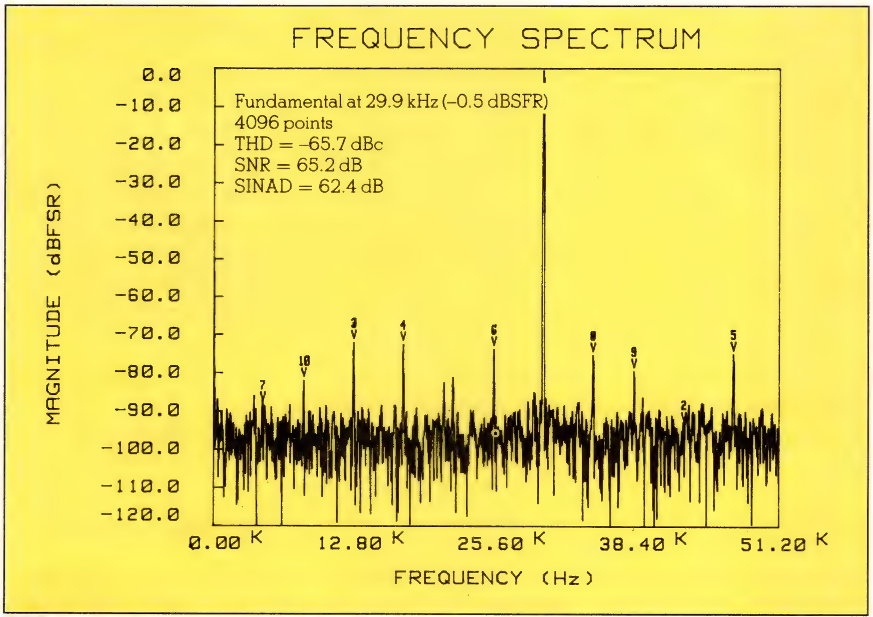
Note that the desire to maintain spectral order after digitizing only increases the required sampling frequency by about 5.5 kHz as compared with using k = 19.

damental appears in the 16.9-kHz bin when sampled at 102.4 kHz, and in the 9.9-kHz bin when sampled at 101 kHz. Solving for various possible input frequencies using Equations 4 and 5 shows that the actual input had to be 495.1 kHz in order for the fundamentals to alias into exactly these two bins for these sampling rates.

As an additional check for both the equations and the spreadsheet, attempts were made empirically to find another input frequency that would result in these two FFTs, but no other input frequencies worked. Note that even at the full 800-kHz maximum-specified sampling rate for the ADS7819, this input frequency is still undersampled, but the performance of the sample-and-hold on the ADC hasn't degraded significantly. Sampling at 800 kHz wouldn't have yielded any additional information about the 495.1-kHz input sine wave, as compared with collecting the data at roughly 25% of that rate using two ADS7819s.

Figures 8 and 9 begin to show one of the real-world limitations previously discussed. Looking at either of these FFT plots raises the question of whether the original input consisted of a single tone near full scale plus additional tones roughly 70 dB below full scale, or whether a single input tone was being distorted by the sampling mechanism. Using Equations 4 and 5, it can be determined that the fundamental bins in these two figures are consistent with a single input tone at 1301.3 kHz. The other lower peaks in the FFT, located in the harmonic bins associated with a 1301.1-kHz input, are consistent with the expected distortion as described in the ADS7819 data sheet for very-high input frequencies.

Comparing Figures 4 and 5 with Figures 8 and 9 points out another real-world limitation to practical undersampling, although this limitation applies not only to the dual-rate sampling approach, but to any undersampling technique. Between these pairs of FFTs, the signal-to-noise ratio (SNR), which excludes harmonics, degrades from slightly above 70 dB to about 65 dB. The prime cause of this degradation is jitter, although it's extremely difficult to determine the relative contributions to jitter from the ADC, the conversion clock generator, and the signal source. Jitter on any of these increases noise in the digitized output of the ADC more at higher input frequencies. That's because the input signal varies more between samples, and jitter is an uncertainty as to the precise time interval between samples.



**8. REAL-WORLD LIMITATIONS** can be detected in this FFT plot of a 1.3013-MHz input sampled at 102.4 kHz. It's hard to tell whether the original input consisted of a single 11.7-kHz tone near full scale plus additional tones roughly 70 dB below full scale, or whether a 1.3013-MHz input tone was being distorted by the sampling mechanism.

In all of the testing discussed to this point, two ADS7819s were used to implement the dual-rate system. However, there's nothing inherent in this approach that requires that the two ADCs need to have similar performance or even the same resolution. The second ADC doesn't add to the accuracy of the system. It's merely used, in combination with the first ADC, to determine how much, if any, aliasing occurred on the actual analog input fundamental. For example, a 16-bit ADC could be employed as the primary converter, and an 8- or 12-bit ADC as the secondary, to optimize system complexity and cost. The main trade-off from using a lower-resolution secondary ADC is that it will limit the dynamic range of the complete system.

## DATA COLLECTION

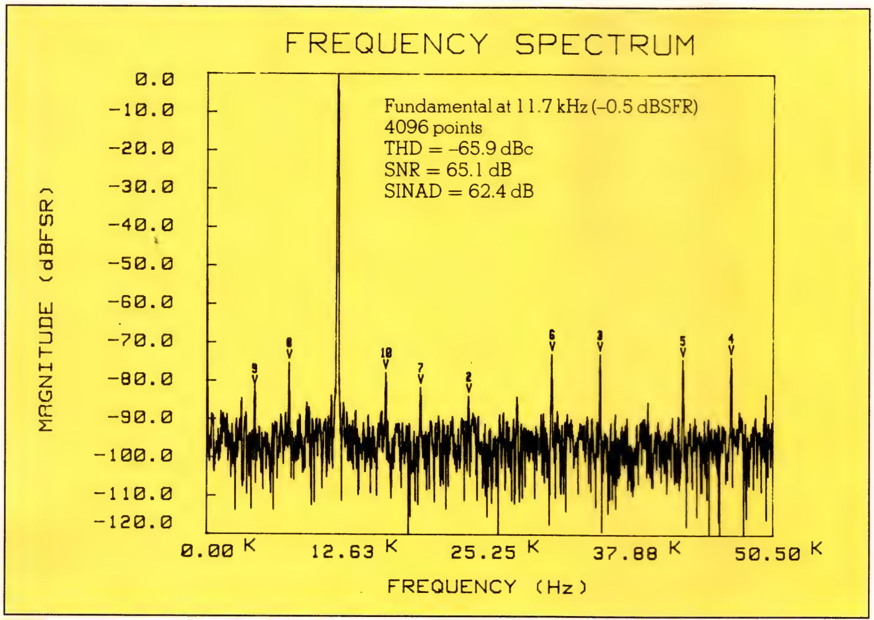
Furthermore, the two ADCs needn't collect an equal number of data points. One could collect as large a number of data points as is practical with the primary ADC, while the secondary ADC would only need to take as many samples as are required to achieve the bandwidth resolution needed. In other words, if the signals to be identified accurately aren't close to each other, then the secondary ADC can capture a very limited number of samples. The number of data points collected from each of the ADCs can be traded off to maximize performance from a given set of digital hardware and software, or to reduce the amount of hardware and software required.

One additional alternative arises if the input signal is continuous: the dual-rate technique could be implemented using a single ADC. One set of data could be collected at the first sample rate, and a second set of data could then be collected at a different sampling rate, again allowing trade-offs between system complexity and cost.

The limitations previously discussed on the dual-rate technique that's related to:

$$\frac{f_{s2} - f_{s1}}{2} \qquad (10)$$

also suggest a way to modify a real system to make it more useful: Designing a system with either a single ADC or dual ADCs, but providing the ability to select from more than two



**9. THE SAME LIMITATIONS** as illustrated in Figure 8 are present when the 1.3013-MHz input is sampled at 101 kHz. The lower peaks in the FFT, located in the harmonic bins associated with a 1301.1-kHz input, are consistent with the expected distortion described in the ADS7819 data sheet for very-high input frequencies.

sampling frequencies, could increase the usefulness of the technique. When one of the potential problem frequencies shows up in any pair of data sets, assuming the input signal is continuous, then one of the alternate sampling frequencies could be used to remove the ambiguity.

Undersampling, like any other concept, carries with it certain limitations that need to be understood in order to use it successfully *(see "How to determine the proper undersampling rate," p. 77)*. One simple limitation for this approach is obvious: the signal that's being digitized must be reasonably continuous and repetitive. Undersampling simply won't work if the signal of interest is a fast pulse, for example. This means that for undersampling to be useful, the signal of interest needs to extend over a reasonably long sampling time.

In the previous example of a 50-kHz bandwidth of interest centered on a 4.975-MHz carrier, it was pointed out that a 100-kHz sample rate can provide the same accuracy as a 10-MHz sampling rate. However, to perform a 1024-point FFT at a 10-MHz sample rate, all of the data is captured in 102.4 µs, while at 100-kHz sample rate it takes 10.24 ms. In some applications, particularly where data needs to be collected as quickly as possible after some triggering event, this delay will be unacceptable because the signal to be digitized will be attenuated.

In such a dual-rate sampling system, which uses two ADCs with different conversion rates, another limitation needs to be considered. In this approach, the digital-processing section needs to perform two complete FFTs, and then compare the results using additional processing steps. While memory sizes and digital-processing performance continue to increase rapidly, and prices continue to decline, the extra software and digital processing required to implement the two-ADC approach needs to be compared with extra costs and development time needed to solve the same problem with a faster ADC. ☐

*George Hill, a development manager in Burr-Brown's Data Div., holds a BS in physics and an MS in political science from Washington University, St. Louis, Mo.*

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|---|---|
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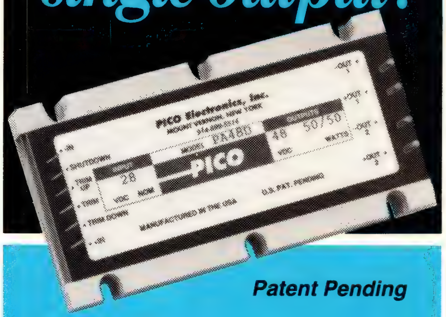
| MODERATELY | 534 |
| SLIGHTLY | 535 |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# USE DSP FILTER CONCEPTS IN IF SYSTEM DESIGN

## COMBINE DIGITAL AND RF DESIGN DOMAINS TO REDUCE SYSTEM NOISE, UP DYNAMIC RANGE, AND SIMPLIFY BASEBAND DSP REQUIREMENTS.

**DAVID B. CHESTER AND GEOFF PHILLIPS**
Harris Semiconductor,
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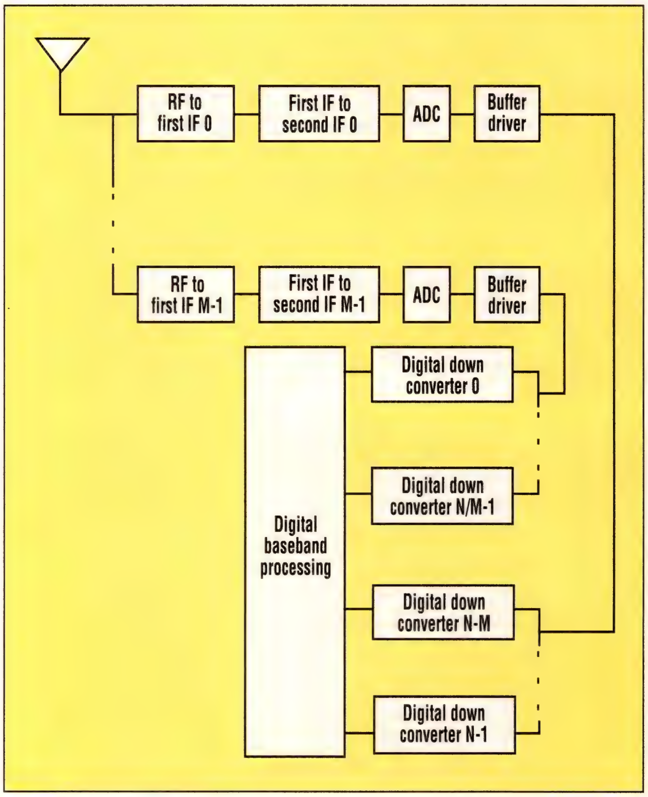
(407) 724-7000.

Industry experts predict that a "wireless decade" is coming in which scores of mainstream digital products will turn to RF for data communication. Many engineers already are taking steps in that direction by applying digital signal processing (DSP) microprocessors to baseband signals. The next step is to move up the frequency spectrum while staying in the digital domain. RF DSP can reduce system noise and increase dynamic range, as well as simplify baseband DSP requirements.

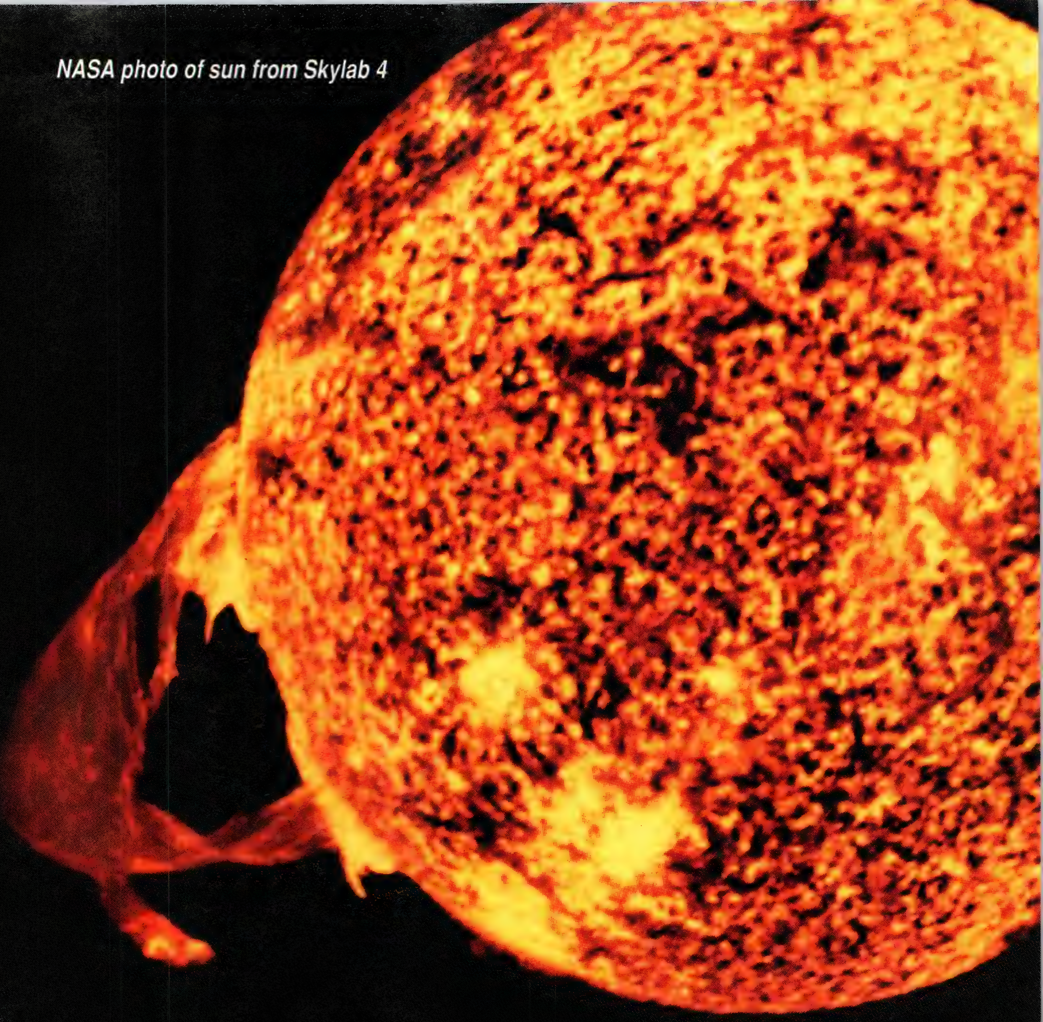
However, the move to RF DSP is a challenging one. RF DSP is new territory not only to engineers used to designing all-digital products, but also to many RF engineers. The technology has only recently emerged from specialized systems into a broader commercial arena, introducing new definitions and new ways of looking at old system-design concepts.

DSP techniques hold many advantages over traditional analog signal processing. Some of these are found in the area of digital filtering. While engineers may be familiar with baseband digital signal processing using software-based DSP microprocessors, the architectures of digital signal microprocessors are usually optimized to perform sum-of-products calculations. They aren't optimized for any specific DSP functions. Maximizing a digital filter's performance requires hardware specifically designed for


RF to first IF 0
First IF to second IF 0
ADC
Buffer driver
RF to first IF M-1
First IF to second IF M-1
ADC
Buffer driver
Digital baseband processing
Digital down converter 0
Digital down converter N/M-1
Digital down converter N-M
Digital down converter N-1

**1. IN A WIDEBAND** wireless base-station receiver, N separate channels are frequency-division multiplexed in the RF spectrum. Each of M signal-processing chains processes a segment of the RF spectrum that contains V/M channels.

NASA photo of sun from Skylab 4



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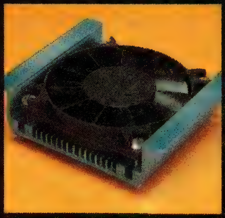

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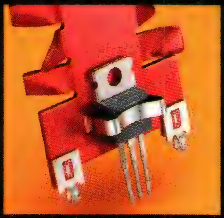

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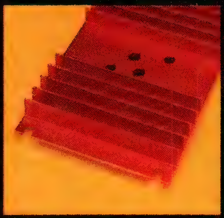

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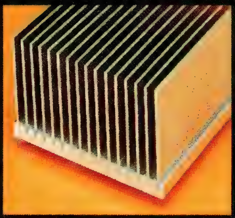

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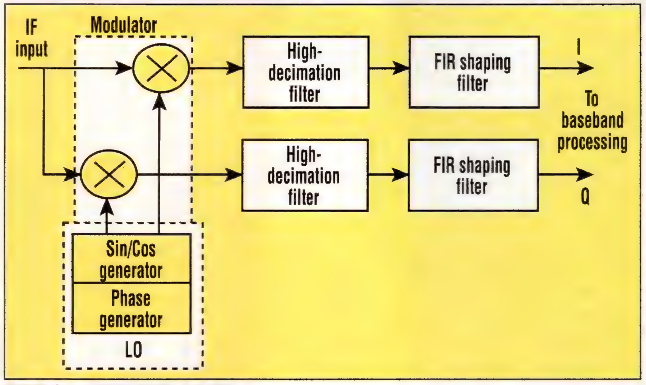
the intended filter function at the desired sampling frequencies.

Although an analog filter is inherently more size- and power-efficient, it's far more component sensitive than its digital counterpart. Digital filters are preferred over analog filters if system requirements call for linear-phase response or an ability to manipulate phase, very high stopband attenuation, very low passband ripple, very low shape factors (the ratio of the filter's passband width plus the filter's transition bandwidth to the filter's passband width), or programmable or adaptive response.



**2. WIDEBAND** digital downconversion can be done by the Harris HSP50016 DDC, a monolithic device that's the digital equivalent of a voltage- controlled oscillator, quadrature mixer, and quadrature filter network. It incorporates a numerically-controlled oscillator-mixer and two decimating filters with in-phase (I) and quadrature (Q) outputs. A DDC clock rate of 75 MHz supports the wideband spectrum.

One of the largest emerging application areas for digital intermediate-frequency (IF) processing is wireless base stations. Most wireless digital-filter applications in base stations are FIR decimation filters in the receive section and FIR interpolation filters in the transmit section. When a digital filter reduces the bandwidth of a signal of interest (meaning the filter output would be oversampled if the input sample rate were preserved), it's computationally efficient to reduce the output sample rate. Decimation is the process of filtering and reducing the output sampling rate by taking every Mth sample. The computational efficiency arises because it's no longer necessary to compute outputs for discarded samples. Thus, there's a one-to-one correspondence between decimation rate and gain in computational efficiency.

Interpolation means increasing the sampling rate. It's most often used when a narrowband signal is combined with a signal that requires a higher sampling rate. Conceptually, the first step in interpolation is to stuff L-1 zero-valued samples between each valid input sample to expand the sampling rate by a factor of L. In the frequency domain, this causes the original signal spectrum to be repeated L-1 times. To perform the actual interpolation, the zero-valued input samples must be converted to approximations of signal samples. This is equivalent to preserving the original signal spectrum. Effectively, the zero-stuffed input stream is filtered by a low-pass filter with a passband at the original spectrum location, which filters out all of the repeated spectra.

Improved computational efficiency is possible in FIR filters used for interpolation because only every Lth data value is non-zero and requires an actual multiply-add operation. Again, there's a one-to-one correspondence between interpolation rate and gain in computational efficiency. This efficient interpolation structure is called polyphase.

Equalization is another important application of high-throughput digital filters in wireless applications. If a channel's characteristics can change as a function of time, the equalization filter's coefficients must be computed in real time to adapt to the channel. Equalization uses a filter with either fixed or time-varying (adaptive equalization) coefficients to reverse the intersymbol interference effect of the communications medium on the signal. Intersymbol interference is usually induced by either multipath effects or channel bandwidth compression.

## WIRELESS BASE STATION

It makes sense to begin examining digital design in wireless base stations with the receiver function. Transmitters will be discussed later.

Digital IF applications in wireless base-station receivers can be broken into two general categories: wideband and narrowband. Wideband receivers first digitize multiple channels at an IF and then digitally separate each baseband channel. They are used in applications such as those that employ the U.S. AMPS standard. AMPS' dynamic range requirements are within the capabilities of cost-effective wideband analog-to-digital converters (ADCs)_for example, 14 bits of resolution at 10 Msamples/s.

In contrast, narrowband digital IF receivers, which employ conventional analog tuning prior to any DSP, are used in applications that employ the European GSM standard, in which the system's dynamic-range requirements only can be met by narrowband processing, but where the processing and manufacturing advantages of digital signal processing are still desirable.

Consider a wideband wireless base-station receiver in which N separate channels are frequency-division multiplexed in the RF spectrum *(Fig. 1)*. Each of the M signal-processing chains processes a segment of the RF spectrum that contains N/M channels. These segments are typically tuned to baseband using two IF stages. The bandpass filter in the second IF can be used as the antialiasing filter that precedes the ADC. The ADC digitizes the baseband signal and passes it to N/M digital downconverters, each tuned to the center frequency of one of the channels. Each digital downconverter centers its channel at dc, performs final shaping, decimates the sampling frequency to make it consistent with the output bandwidth, and outputs a quadrature data stream. The output of each digital downconverter is passed to a digital baseband processing unit, which demodulates, decodes, and routes the signal. Each baseband channel may have its own dedicated post-processing circuitry, or it may share resources among multiple channels.

A practical wideband receiver might simultaneously receive 60 channels, each 30-kHz wide, with the channel center frequencies separated by 210 kHz. Further requirements could include an ADC with 80-dB single-tone spurious free dynamic range

(SFDR), and a demodulator with 20-dB signal-to-noise ratio (SNR) at its input. The weakest signal to be received might be 70 dB below full-scale through the ADC.

Assume that a system trade study has dictated a system configuration with six parallel signal-processing chains (M = 6), each processing 10 channels, and a 45-ksample/s quadrature-output baseband sampling frequency.

Each analog-processing chain brings its band of interest to a 2.25-MHz center frequency. The baseband signal input to the ADCs extends from 1.29 to 3.31 MHz. To provide a reasonably flat amplitude and group-delay response in the band of interest while allowing for a reasonable shape factor and sampling rate, the 3-dB points chosen for the antialias filters in the analog IF stages are 0.97 MHz and 3.63 MHz.

To preserve the required SFDR, the filter must provide 80 dB of attenuation at –1.09 MHz and 5.69 MHz (the digital sampled data folding frequencies are 0 Hz and $f_s/2$). These parameters provide a filter shape factor of approximately 2.5. The filtered signal is sampled at a rate of 9 Msamples/s and distributed to 10 digital downconverters.

For maximum end-to-end system performance, assume that the noise floor of the analog front end is at the same level as the noise floor of the ADC. A typical 14-bit ADC has greater than 80-dB SFDR (meeting the specified system requirements), and approximately 72- to 74-dB SNR. Thus, the SNR into the digital downconverter is assumed to be 70 dB.

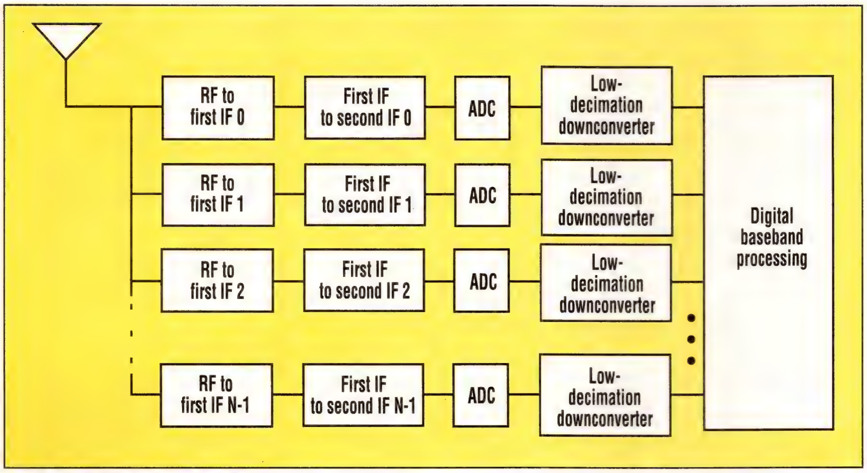
## DOWNCONVERSION

A digital downconverter has a number of advantages over an analog downconverter: arbitrarily precise tuning, arbitrarily large SFDR and SNR, linear-phase filter characteristics, sharp filter roll-off, small passband ripple, large stopband attenuation, no parameter drift with time or temperature, and ease of manufacturability *(Fig. 2)*. The block diagram shown is similar to that of the Harris HSP50016 DDC.[1]

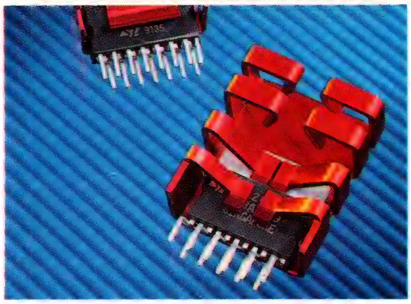
The downconverter first mixes the input signal by means of a quadrature local oscillator (LO) to center the channel of interest at dc. In this example, the 10 downconverters per processing chain would be set with LO frequencies separated by 210 kHz, beginning at 1.305 MHz. After mixing, the downconverter quadrature lowpass filters and decimates the dc-centered complex result.

Conceptually, a quadrature filter is two identical real filters, one filtering the real data stream of a complex signal and the other filtering the imaginary data stream. To clarify our terminology, a complex signal can have a two-sided spectrum (that is, two sidebands, as opposed to positive and negative frequency components), whereas a quadrature signal is always a complex signal with a one-sided spectrum.

The desired quadrature output


RF to first IF 0
First IF to second IF 0
ADC
Low-decimation downconverter
RF to first IF 1
First IF to second IF 1
ADC
Low-decimation downconverter
RF to first IF 2
First IF to second IF 2
ADC
Low-decimation downconverter
RF to first IF N-1
First IF to second IF N-1
ADC
Low-decimation downconverter
Digital baseband processing

**3. A WIRELESS** base-station receiver using narrowband digital IF processing employs N separate information channels, which are frequency-division multiplexed in the RF spectrum. An analog processing chain and ADC are dedicated to each of the N channels.



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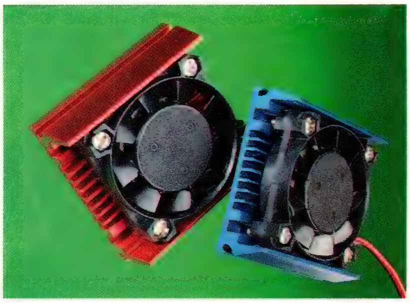

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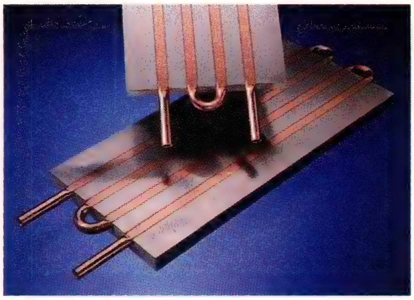

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sampling rate of 45 ksamples/s requires a decimation rate of 200. Because of this relatively high decimation rate, the filtering is most efficiently performed in two stages. In these high decimation-rate cases, it's common to use a multiplier-free high decimation filter as the first stage, and a traditional FIR as the second stage.[1,2,3] In this example, the high decimation filter decimates by a factor of 50. The FIR then performs final shaping on the band of interest, giving it a 30-kHz bandwidth, and decimates by a factor of 4. Both filters have linear-phase characteristics.

In general, the process of low-pass filtering has no effect on SFDR. The worst-case spur produced by the analog front-end or ADC may lie in one of the channels of interest. Thus, the digital downconverter can't guarantee an improvement in SFDR. SNR, however, is improved in the digital downconverter, assuming that it's designed to have a noise floor below the input-noise floor. Given uniformly distributed noise, SNR improves by three decibels every time the input bandwidth is reduced by a factor of two. In this example, the single-sided noise bandwidth of the input to the digital downconverter is 4.5 MHz, and the output noise bandwidth is 30 kHz. This results in approximately a 22-dB improvement in SNR.

For a worst-case channel, where the signal of interest is down 70 dB from full-scale, the signal-to-wideband-noise ratio is 0 dB. Because of the processing, the SNR out of the digital downconverter is 22 dB, 2 dB better than the specification required.

As noted earlier, narrowband digital IF processing is used in applications such as the European GSM cellular telephony standard *(Fig. 3)*. Narrowband is an analog/digital compromise dictated by the near-far problem and the limitations of today's ADC technology. The classic example of the near-far problem is the case in which one mobile unit is located close to the base station while another resides at the edge of the cell, causing a large difference in received power at the base station. To deal with this, GSM requires a large wideband dynamic range, on the order of 110 dB. Within any one channel however, the dynamic

## DESIGNING DIGITAL FILTERS

Most engineers are comfortable with the time domain when conceptualizing the operation of an analog filter. However, a digital filter is better conceptualized in the frequency domain. Digital filters simply perform a convolution of the time-domain impulse response and the sampled signal. A filter is designed by choosing a frequency-domain impulse response, transforming it into a time-domain impulse response, and finally converting it to the filter's coefficients.

Another reason for thinking in the frequency domain is the reality that digital filtering is essentially a mathematical process. Although the characteristics of an analog filter are directly attributable to the physics of the device that implements it, the characteristics of a digital filter are only indirectly attributable to physics. In other words, a digital filter's passband ripple, shape factor, stopband attenuation, and phase characteristics are all functions of the order and type of polynomial used to approximate the ideal impulse response, the number of bits used in performing the arithmetic, and the type of architecture used to implement the arithmetic.

Actual frequencies have no meaning in a digital filter except in their relation to the sampling frequency, because the impulse response is generated as a function of $z^{-1}$, called the sample interval (the time between samples). For a smaller shape factor, the order of the filter and the number of bits in the arithmetic can be increased. Basically, the only physical limitation is the amount of arithmetic processing that can be integrated on a device or devices given the filter order and the input sampling rate.

The two types of digital filters are finite impulse response (FIR) and infinite impulse response (IIR). With an FIR, the filter is excited with an impulse, and the output is present for a finite number of computational cycles (N, the length of the filter). An FIR filter has no feedback coefficients, only feedforward coefficients.

An IIR filter, on the other hand, has one or more non-zero feedback coefficients. The feedback term(s) mean there's always an output once the filter is excited.

Because an IIR filter uses both a feedforward polynomial (zeros as the roots) and a feedback polynomial (poles as the roots), it has a sharper transition characteristic for any given filter order. Like an analog filter with poles, an IIR filter usually has nonlinear phase characteristics. Also, the feedback loop makes it difficult to use in adaptive filter applications.

FIR filters are clearly the filter of choice in wireless base-station applications. One reason is that, because of its structure, when the filter's coefficients are symmetric, an FIR filter has a linear-phase response. This is the case in most standard filtering applications. Also, an FIR's implementation noise characteristics are easy to model, especially if intermediate truncation isn't used.

An IIR filter's poles may be close to or outside the unit circle in the Z-plane. This means an IIR filter may have stability problems, especially after quantization is applied. An FIR filter is always stable. Finally, FIR filters allow development of computationally efficient architectures in decimation or interpolation applications.

Typically there are three stages to designing digital-filter responses for passband filters. First, specify the ideal filter response. Next, design a floating-point response. Lastly, quantize the floating-point coefficients to yield a fixed-point response.

The specification for the ideal filter includes the location of passbands and stopbands, minimum stopband attenuation, maximum passband ripple, filter order, and perhaps the shape of the response in some of the specified bands. The range requirement is on the order of 50 dB, well within the capabilities of current ADC technology.

As shown in Figure 3, each of the N signal-processing chains typically has two analog IF stages. In this example, the first processing stage tunes one of N frequency-division multiplex channels in the cell to a fixed first IF. The second IF-processing stage translates the channel of interest to a fixed second IF. The bandpass filtering in the analog IF-processing stages acts as the antialiasing filter for the ADC.

The actual location of the second IF is a trade-off between the bandpass filters, the desired processing gain that occurs in the digital downconversion, and the performance characteristics of the ADC. If the IF is at baseband, a low-speed ADC could be used, but the bandpass filter might be costly because of the low frequencies involved. If a higher IF were used, the cost of the bandpass antialiasing filter could be reduced. Also, the digital filter would reject more of the input-noise bandwidth, thus increasing processing gain. With the higher IF, however, the ADC must be able to digitize the higher-frequency signal. Even if subsampling were used, the dynamic performance of the front-end of the ADC would have to be consistent with the higher second IF.

The sampling frequency of the ADC must be an integer multiple of the required baseband sampling rate. For GSM, this is 270.833 quadrature ksample/s.

To illustrate the subsampling technique, choose the frequency of the second IF to be 6.5 MHz and the ADC sampling frequency to be 8.666 Msamples/s. The GSM double-sided passband is approximately 180 kHz, so the bandpass filter must have linear-phase characteristics in that region. Also, the antialiasing filter must have roll-off characteristics that preclude unwanted aliasing. Subsampling, of course, is the desired aliasing.

After being digitized by the ADC, the IF is spectrally reversed and centered at 2.166 MHz ($f_s/4$, or one-quarter of the sampling frequency). This trivializes the design of the LO and mixer in the low-decimation downconverter. Therefore, in this case, the device performing that function need only be a slightly modified quadrature low-decimation filter. The digital downconverter in Figure 3 is labeled a low-decimation downconverter to highlight its architectural difference from the high-decimation digital downconverter used in wideband applications.

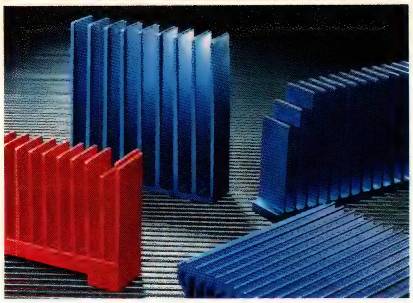
The LO generates a quadrature sinusoid at a frequency of $+f_s/4$. The plus sign induces another spectral reversal (the lower sideband of the real input is centered at dc) to spectrally normalize the dc-centered signal. The in-phase part of the LO is 1, 0, –1, 0, . . . and the quadrature-phase part of the LO is 0, 1, 0, –1, . . .

In addition to requiring only a trivial LO, the low-decimation filter performs a quadrature low-pass filtering

common methods of designing floating-point FIR filter responses are the windowing, frequency-sampling, and optimal methods.

Converting floating-point coefficients into fixed-point coefficients requires quantizing the coefficients and calculating the frequency-domain impulse response of the filter or filter model to verify that the filter meets the required specification. If it doesn't, one of three things must happen: the number of coefficient bits can be increased, the filter response can be redefined, and the second step of the process repeated; the filter arithmetic can be redesigned; or a combination of these procedures can be performed. When filter hardware is at a premium, sophisticated simulated-annealing techniques help find the best set of filter coefficients, given a fixed filter order and coefficient width.

Coefficients for adaptive filter responses are computed using special algorithms that constantly recalculate coefficient values based on the error characteristics of received data. While the coefficient calculation method for an adaptive filter is different than those described above for a passband filter, the actual filter structures are the same, except that coefficients must be changed in real time.



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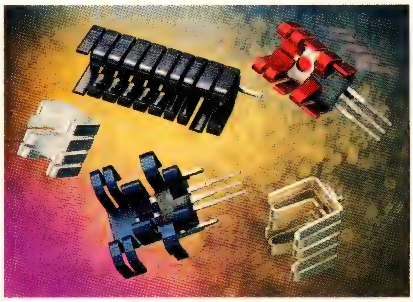

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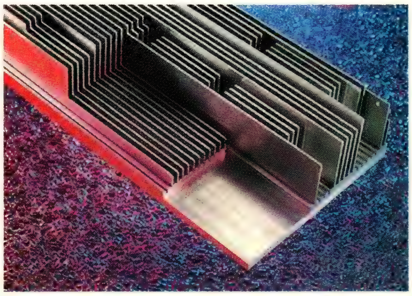

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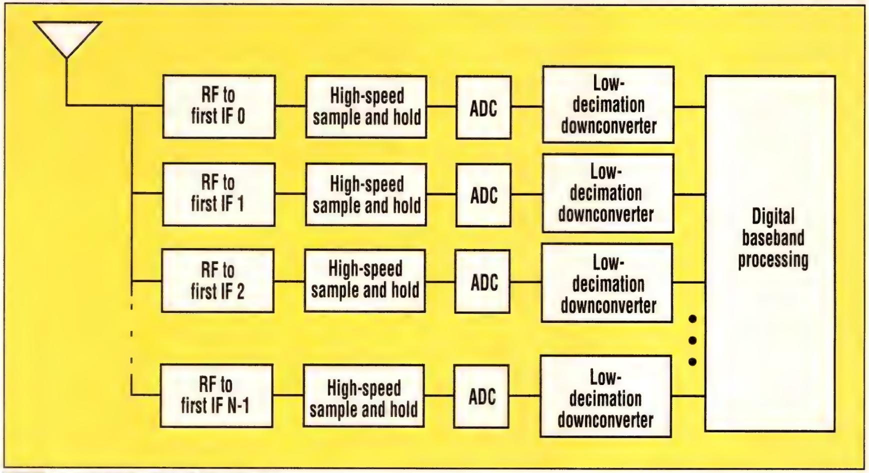
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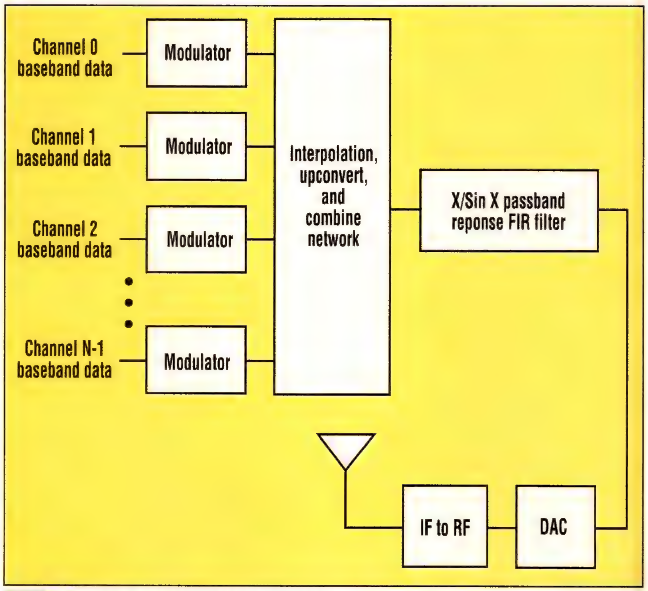
RF to first IF 2
High-speed sample and hold
ADC
Low-decimation downconverter
RF to first IF N-1
High-speed sample and hold
ADC
Low-decimation downconverter
Digital baseband processing

**4. THE SINGLE-IF** narrowband receiver is a derivative of the architecture shown in Figure 3. In this case, however, a high degree of subsampling brings the channel of interest from the first IF to baseband. This configuration trades a second analog IF-processing stage for a high-speed sample-and-hold (or track-and-hold) in front of the ADC.

operation and decimates the I and Q components of the quadrature result by a factor of 32. This produces the desired output sampling rate.

A decimation rate of 32 is too low to justify the use of a high-decimation filter architecture like the one used in the wideband approach. Instead, one of many classic multistage FIR structures[3] can be used to provide final shaping to the GSM specification and decimation.

The single-sided noise bandwidth into the low-decimation filter is 4.333 MHz, and the output noise bandwidth is 180 kHz. This results in a processing gain of approximately 14 dB. As in the wideband design, the resultant quadrature data is passed to digital baseband-processing circuitry for final processing.



**5. IN A DISTRIBUTED** digital multichannel transmitter, the first major function is encoding and modulating the baseband data of each channel. The modulation is performed at a sampling rate consistent with the baseband data rate.

## ONE IF STAGE

A digital, narrowband, wireless receiver also can be made with just a single analog IF processing stage *(Fig. 4)*. The first IF processing stage tunes a frequency-division multiplexed channel of interest to a fixed IF. The IF is selected on the basis of the ADC sampling frequency and the characteristics of the bandpass antialiasing filter in the IF processing stage. A high-speed sample-and-hold then captures samples of the IF signal at a subsampling rate.

As an example, consider a sampling frequency of 4.333 Msamples/s and a first IF of 70.4 MHz. The passband of interest extends from 70.31 MHz to 70.49 MHz. The Nyquist folding frequencies for the antialias bandpass filter are 69.333 MHz and 71.5 MHz. The antialias bandpass filter must have linear phase and flat amplitude characteristics in the area of the passband of interest and must roll off the desired attenuation (on the order of 100 dB) by the time the filter folds back into the passband of interest. This occurs at 68.356 MHz and 72.51 MHz.

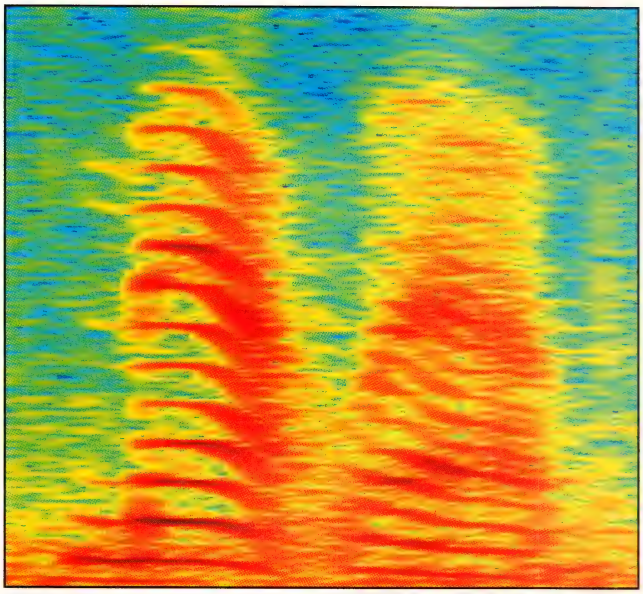
Designing the sample-and-hold is challenging because the circuit must provide an aperture time and aperture jitter that yields the desired SFDR at the IF while affording a hold time consistent with the ADC sampling frequency. In this example, the required aperture time is on the order of 1 ps while the hold time is on the order of 200 ns.

After being subsampled by the ADC, the IF center frequency is constructively aliased to 1.067 MHz with a normal (not reversed) spectral sense. Because this center frequency isn't exactly the $f_s/4$ frequency of 1.083 MHz, the LO and mixing operation in the quadrature low decimation downconverter must be performed by a true LO and mixer. If an IF of 70.416 MHz were chosen, the trivial $f_s/4$ LO and mixer could be used. The sampled data is dc-centered by the quadrature mixing process and passed to quadrature low-pass filters for final shaping and decimation by 16.

In this example, the single-sided noise bandwidth into the low-decimation filter circuit is 2.166 MHz. The output noise bandwidth is again 180 kHz. This results in approximately an 11-dB processing gain.

On the transmit side of a wireless base station, multiple baseband signals are upconverted to different RF carrier frequencies and transmitted. Due to the engineering economics of the system, this is typically accomplished by first converting the baseband signals to IF frequencies, where the IFs are separated in frequency by the final desired frequency separation, and combining the individual IF signals into a composite IF signal.

The baseband data is inherently digital. If the entire upconversion and combining process is to be performed using analog circuit techniques, the baseband data first must be converted to analog format. Modulating the binary data is most likely accomplished in some form of digital baseband processor. The modulation is performed at a sampling rate



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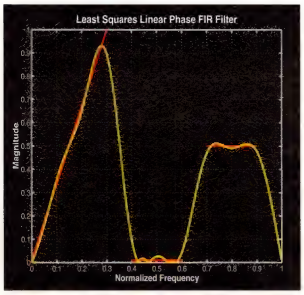

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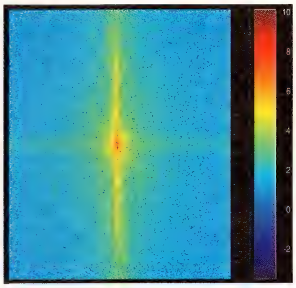

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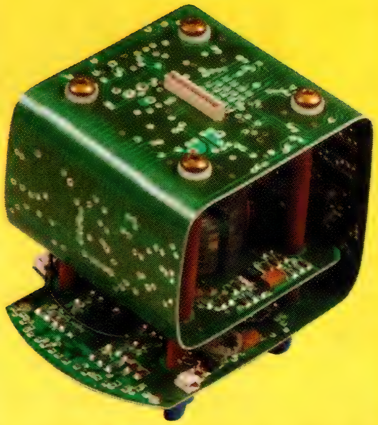

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consistent with the baseband data rate. The digital baseband-modulated sampled data stream is then converted to analog format using a digital-to-analog converter (DAC).

The baseband analog signals are upconverted to an IF and the individual IF signals are added. The composite IF is upconverted to the desired RF frequency and transmitted. This requires multiple DACs, smoothing filters, and upconverters, and a large analog summing tree.

While variations on this configuration may reduce the number of analog signals (by combining multiple digital modulated channels in the baseband processor, for example), multiple analog-processing chains are very difficult and costly to implement, given the severe performance specifications of a cellular base station. Spurious signals arise in the digital-to-analog conversion process and at each analog-signal-processing step. Costly components, design techniques, and manufacturing methods are needed to provide the required performance.

## DSP TECHNIQUES

DSP techniques can circumvent a number of the problems associated with the analog-signal-processing implementation *(Fig. 5)*. Modulation takes place at a smapling rate consistent with the data rate. Once the data is in a modulated form, the sampling rate must be raised to a rate that allows it to be upconverted and combined in a frequency-division multiplex sense to form a composite IF signal. Each interpolated baseband channel is then upconverted to a different IF separated by the desired RF frequency-division multiplex spacing. There are many actual implementations with which it's possible to perform these processes. For example, modulation and interpolation can be combined into a single filtering step. This would be followed by an upconverter and summation tree.

Other possible implementations would begin with a baseband process that generates a quadrature-modulated signal. The quadrature baseband signal would then be passed through a quadrature FIR shaping filter, followed by a multiplier-free quadrature high-interpolation filter. The resulting interpolated signal would then be upconverted by a quadrature LO, and the real part of the result taken (this is basically the transposition of the operation performed by the Harris HSP50016). The real result would then be passed to a summation tree to form a composite IF signal. The baseband quadrature- modulated signal also could be passed to a polyphase generalized discrete-Fourier-transform filter bank structure.[3] This structure would perform the interpolation, upconversion, and summation process.

After the composite IF signal is formed, it's passed to an FIR compensation filter, where the passband is shaped with an (X/Sin X) frequency response to compensate for the (Sin X/X) response of the DAC that follows the filter. The digital compensation filter eases the requirement for the analog smoothing filter. The DAC's output is passed to the analog upconvert and transmit circuitry, which converts the composite IF signal to the desired transmit frequency and supplies the required transmit power. ☐

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*Geoff Phillips, Harris' vice president of engineering, holds a degree from Newcastle Polytechnic, U.K.*

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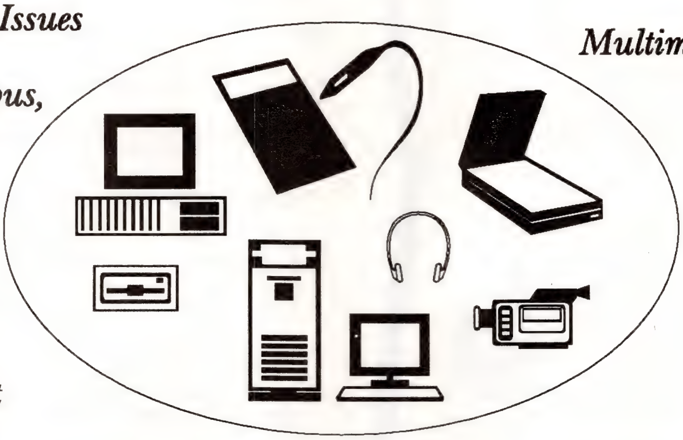

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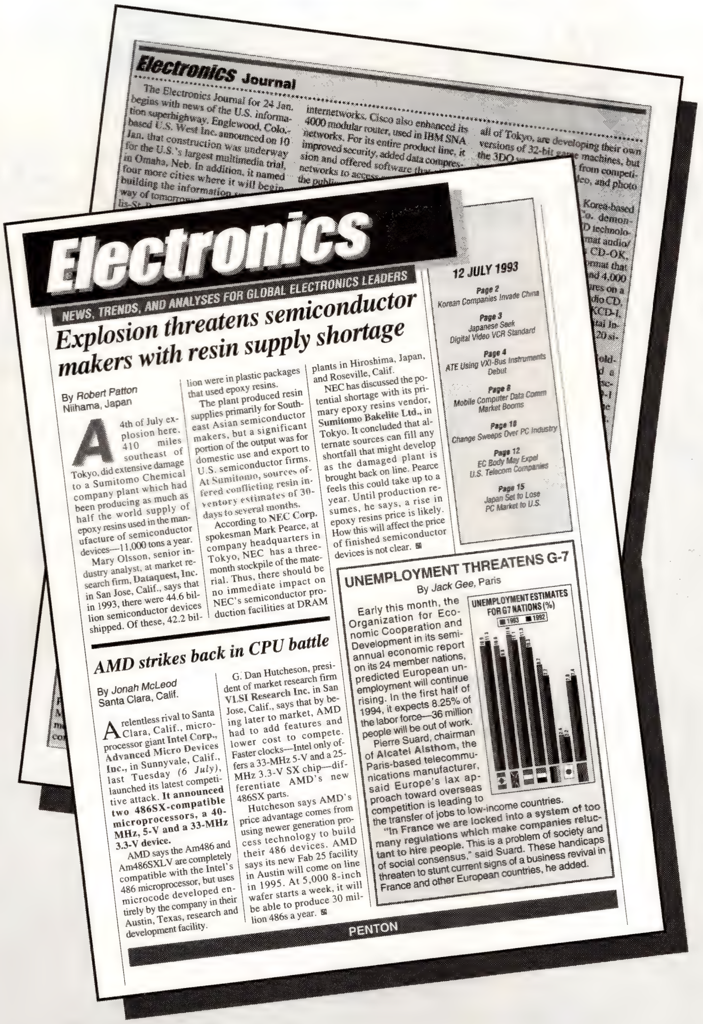

**Electronics Journal**

The Electronics Journal for 24 Jan. begins with news of the U.S. information superhighway. Englewood, Colo.-based U.S. West Inc. announced on 10 Jan. that construction was underway for the U.S.'s largest multimedia trial, in Omaha, Neb. In addition, it named four more cities where it will begin building the information

internetworks. Cisco also enhanced its 4000 modular router, used in IBM SNA networks. For its entire product line, it improved security, added data compression and offered software

**Electronics**

NEWS, TRENDS, AND ANALYSES FOR GLOBAL ELECTRONICS LEADERS

12 JULY 1993

## *Explosion threatens semiconductor makers with resin supply shortage*

By *Robert Patton*
Niihama, Japan

A 4th of July explosion here, 410 miles southeast of Tokyo, did extensive damage to a Sumitomo Chemical company plant which had been producing as much as half the world supply of epoxy resins used in the manufacture of semiconductor devices—11,000 tons a year.

Mary Olsson, senior industry analyst, at market research firm, **Dataquest, Inc.** in San Jose, Calif., says that in 1993, there were 44.6 billion semiconductor devices shipped. Of these, 42.2 billion were in plastic packages that used epoxy resins.

The plant produced resin supplies primarily for Southeast Asian semiconductor makers, but a significant portion of the output was for domestic use and export to U.S. semiconductor firms. At Sumitomo, sources offered conflicting resin inventory estimates of 30-days to several months.

According to **NEC Corp.** spokesman Mark Pearce, at company headquarters in Tokyo, NEC has a three-month stockpile of the material. Thus, there should be no immediate impact on NEC's semiconductor production facilities at DRAM plants in Hiroshima, Japan, and Roseville, Calif.

NEC has discussed the potential shortage with its primary epoxy resins vendor, **Sumitomo Bakelite Ltd.**, in Tokyo. It concluded that alternate sources can fill any shortfall that might develop as the damaged plant is brought back on line. Pearce feels this could take up to a year. Until production resumes, he says, a rise in epoxy resins price is likely. How this will affect the price of finished semiconductor devices is not clear.

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*Korean Companies Invade China*

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*Japan Set to Lose PC Market to U.S.*

## *AMD strikes back in CPU battle*

By *Jonah McLeod*
Santa Clara, Calif.

A relentless rival to Santa Clara, Calif., microprocessor giant **Intel Corp.**, **Advanced Micro Devices Inc.**, in Sunnyvale, Calif., last Tuesday *(6 July)*, launched its latest competitive attack. **It announced two 486SX-compatible microprocessors, a 40-MHz, 5-V and a 33-MHz 3.3-V device.**

AMD says the Am486 and Am486SXLV are completely compatible with the Intel's 486 microprocessor, but uses microcode developed entirely by the company in their Austin, Texas, research and development facility.

G. Dan Hutcheson, president of market research firm **VLSI Research Inc.** in San Jose, Calif., says that by being later to market, AMD had to add features and lower cost to compete. Faster clocks—Intel only offers a 33-MHz 5-V and a 25-MHz 3.3-V SX chip—differentiate AMD's new 486SX parts.

Hutcheson says AMD's price advantage comes from using newer generation process technology to build their 486 devices. AMD says its new Fab 25 facility in Austin will come on line in 1995. At 5,000 8-inch wafer starts a week, it will be able to produce 30 million 486s a year.

## UNEMPLOYMENT THREATENS G-7

By *Jack Gee*, Paris

Early this month, the Organization for Economic Cooperation and Development in its semiannual economic report on its 24 member nations, predicted European unemployment will continue rising. In the first half of 1994, it expects 8.25% of the labor force—36 million people will be out of work.

Pierre Suard, chairman of **Alcatel Alsthom**, the Paris-based telecommunications manufacturer, said Europe's lax approach toward overseas competition is leading to the transfer of jobs to low-income countries.

"In France we are locked into a system of too many regulations which make companies reluctant to hire people. This is a problem of society and of social consensus," said Suard. These handicaps threaten to stunt current signs of a business revival in France and other European countries, he added.

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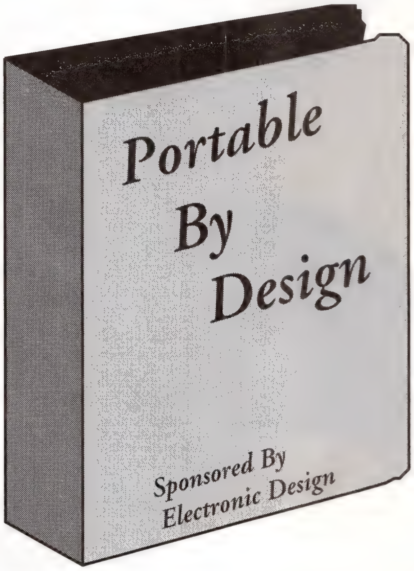

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# TEMP CONTROLLER SWITCHES TRIAC

**JOE BUXTON and DEREK BOWERS**
Analog Devices Inc., Precision Monolithics Div., 1500 Space Park Dr.,
Santa Clara, CA 95052.

The simple circuit shown can turn a heating element on and off when the temperature of the system it's implemented in crosses a user set limit *(see the figure)*. However, the circuit certainly isn't limited to the switching of a heating element—just about any arbitrary device can be substituted as the controlled element.

In the setup, the heating element is connected directly across the ac power line, and a triac is used as the main switch. A triac is ideal because it can handle bidirectional current at reasonably high levels (up to approximately 40 A), and needs only a low-energy signal applied to its gate terminal to turn it on. The signal is supplied by an optically isolated triac driver, the MOC3012.

The actual temperature sensor/controller (the TMP-01) is a monolithic device whose low power allows it to operate with a simple half-wave rectified power supply directly from the ac line. Such an arrangement greatly simplifies the power-supply design requirement to the point of only needing a few low-cost components to provide a single +6-V dc supply.

In fact, this supply design is useful for many low-power, single-supply circuits other than the TMP-01.

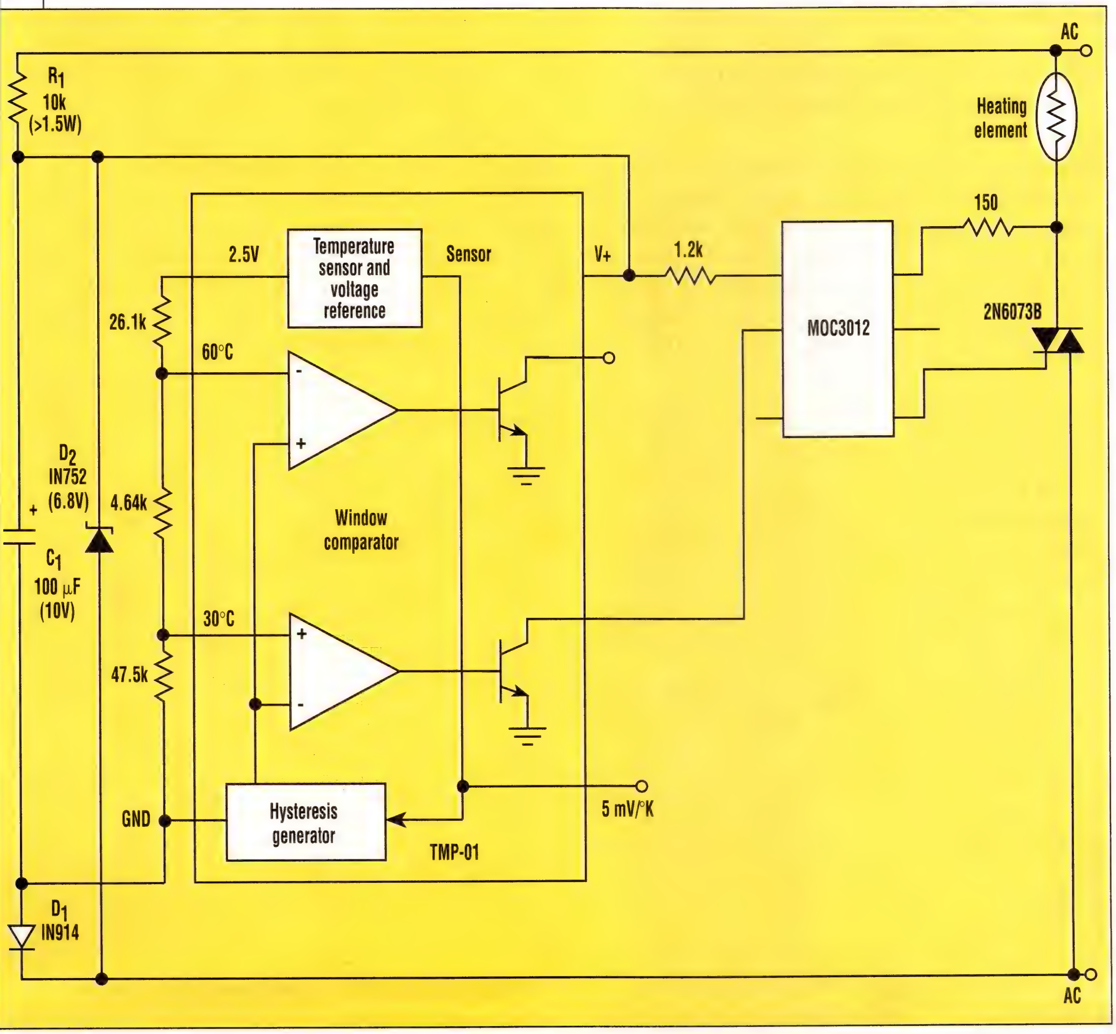
The TMP-01 is essentially a "thermostat on a chip." It includes a linear temperature sensor (5 mV/K), and also has two comparators that switch at externally determined set points. These set points are established by resistively dividing the internal 2.5-V reference to set appropriate voltages on the inputs to the comparators.

One comparator is employed in this circuit to turn on the heating element when the temperature drops below 30°C. With a temperature constant of 5 mV/K, 30°C corresponds to a voltage of 1.52 V on the comparator's input.

This temperature was arbitrarily chosen for the purpose of testing this circuit and could certainly be adjusted to any value within the temperature range of the part. Furthermore, the second comparator could just as easily have been configured to turn on a cooling system as the temperature rose above a certain set point.

When the temperature is below 30°C, the comparator is "on," pulling the open collector output low. This turns on the LED within the MOC3012, energizing the triac.

Above 30°C, the open collector is high, and the LED and triac are off. The MOC3012 was chosen because it requires only 5 mA to energize its LED,



**WHEN THE temperature of a system crosses a user-set limit, this circuit can turn a heating element on or off. The element is connected directly across an ac power line.**

and a lower current is preferable since it reduces the demands put on the power supply.

To provide a dc power supply to the TMP-01, the ac power is half-wave rectified by the two diodes, D1 and D2, and the 10-kΩ resistor $R_1$. On the positive cycle of the 60-Hz line voltage, D2 clamps the voltage across the TMP-01 to 6.8 V minus the diode drop of D1, or about 6.1 V total. Concurrently, capacitor $C_1$ maintains the 6.1 V across the TMP-01. D1 also prevents the reverse voltage from energizing the TMP-01's internal substrate junctions, which could damage the device.

The dc voltage that is held on capacitor $C_1$ will droop due to the current drain of the TMP-01 and the triac controller. However, this drain is small enough to keep the ripple on the dc power line to a value of less than 400 mV p-p.

When the LED within the MOC3012 is turned off, the current demand is much less and the supply ripple drops to 40 mV p-p. In either case, the supply ripple is at a low enough frequency (60 Hz) to be almost entirely rejected by the TMP-01's PSRR of 65 dB. Looking at the reference output of the TMP-01, the ripple is undetectable on an oscilloscope.

This technique for generating a simple supply is useful not only for this type of circuit, but for many others that require a single, low-power supply.☐

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521

# GENERATE STEPPER-MOTOR PULSES

M.S. NAGARAJ
I.S.R.O. Satellite Centre, Digital Systems Div., Airport Rd.,
Vimanapura P.O., Bangalore 580 017, India.

When a stepper motor is controlled manually to move its load over a large distance, the motor drive circuit must be supplied with a continuous clock to move the load quickly to its approximate position. In addition, it must be provided with single-shot pulses for placing the load in the exact position.

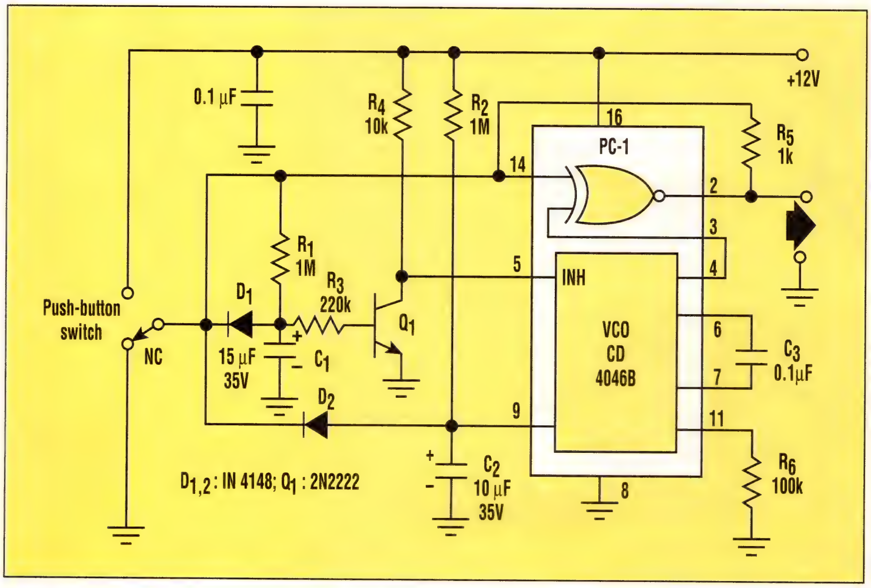
The simple circuit depicted in the figure fills those needs. The circuit, built around a CMOS phase-locked loop IC, CD 4046B, enables a push-button switch to generate not only the switch-debounced one-shot pulses, but also the continuous clock.

When the switch is in its normally-closed (NC) position, capacitors $C_1$ and $C_2$ are held discharged by diodes D1 and D2. Switching off transistor Q1 inhibits the voltage-controlled oscillator of the PLL. The two inputs and, hence, the output of the EX-OR gate (phase comparator 1) of the PLL remain at the logic 0 level.

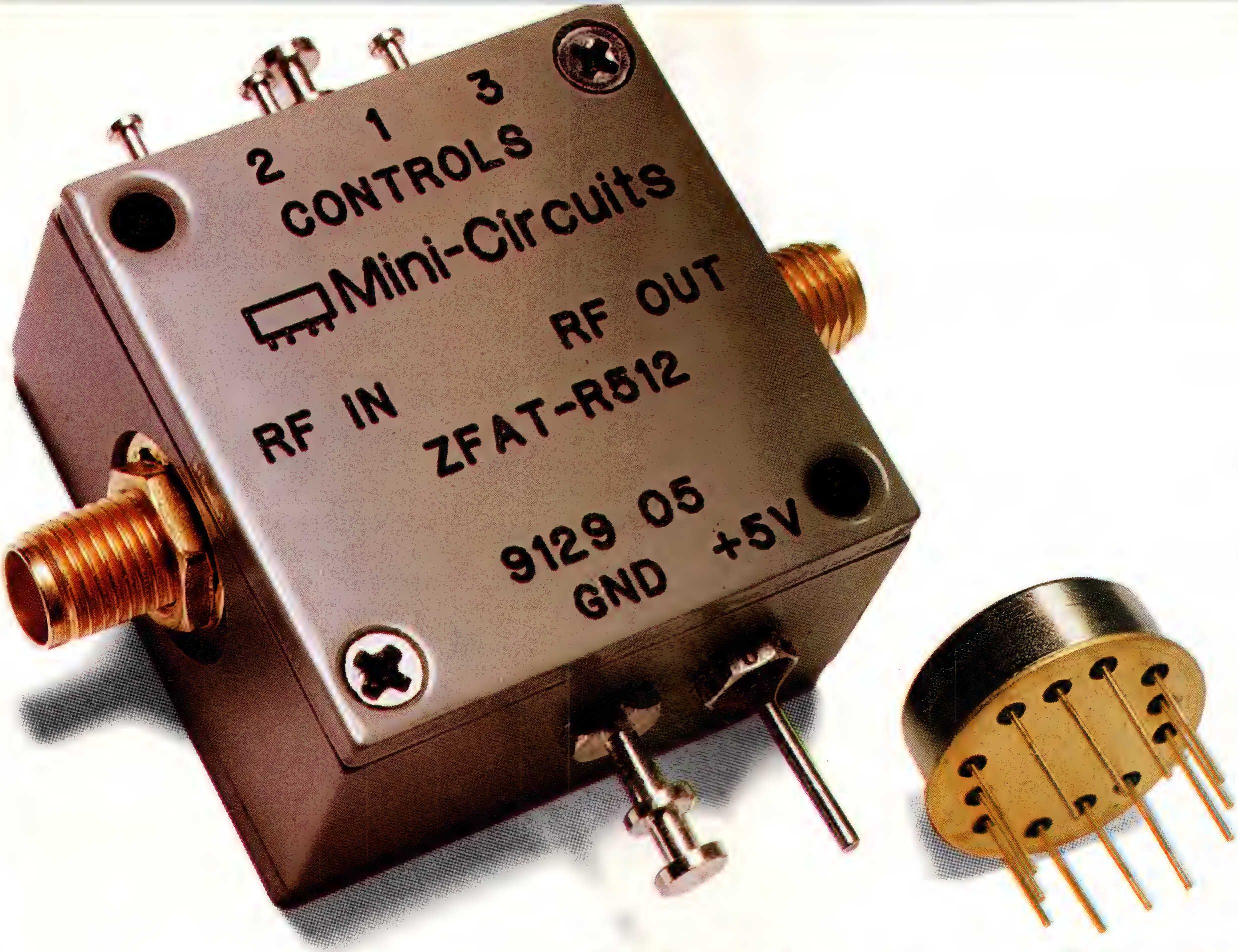
When the push-button is pressed, $C_1$ and $C_2$ are allowed to charge via resistors $R_1$ and $R_2$. The VCO is enabled only after a time delay (≈ 0.5 seconds) set by $R_1$, $R_3$, and $C_1$. During this delay period, the EX-OR gate output follows the logic level at the switch output. As a result, one-shot pulses can be generated by pressing the push-button and then releasing it within 0.5 seconds. $R_5$ provides the switch-debouncing function.

If the push-button is pressed for more than 0.5 seconds, the VCO is enabled. The rising voltage at the control input (pin 9) causes a linear increase in VCO frequency and thus accelerates the stepper motor. Releasing the push-button discharges $C_1$ and $C_2$ and inhibits the VCO.

Components $R_6$ and $C_3$ can be selected so that when the voltage at the control input of the VCO reaches saturation, the VCO oscillates at a frequency equal to the motor's maximum stepping rate.☐



**SWITCH-DEBOUNCED ONE-SHOT PULSES** can be generated for a stepper motor using this circuit. It also produces a continuous clock.



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# 522 ADD ERROR CHECK TO MASTER-SLAVE DEVICE

**M. RAILESHA**
World Friends, Design Group, Kalpakkam 603102, Tamilnadu, India; phone: 0091-4117-508.

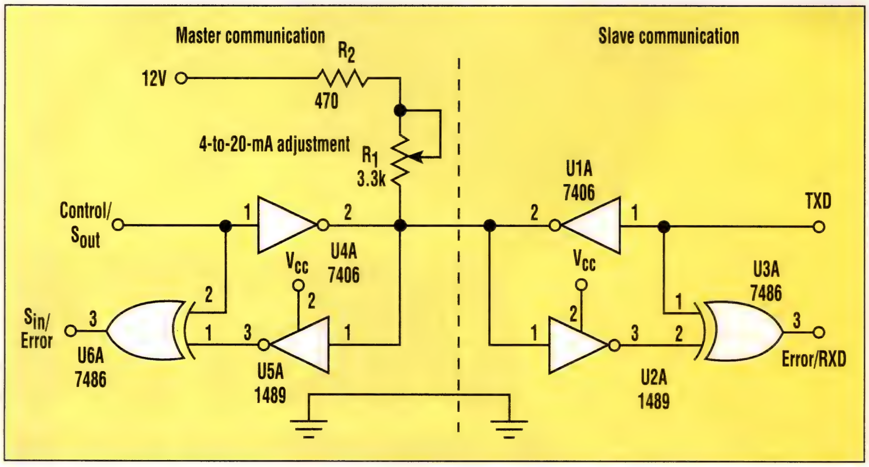
Half-duplex communication, which requires only two electrical conductors, was popular in devices such as teletypewriters, running at 10 characters/s. Even today, designers prefer master-slave communications based on a 0-to-20-mA current loop in half-duplex mode (but at much faster speeds than the teletypewreiters).

An error-check mechanism introduced into master and slave communication devices can be easily monitored by the data-transmitting device *(see the figure)*. Errors generally occur when both the master and slave start sending data simultaneously over the line. The error flag goes high and indicates a mismatch in the data.

The master is the one that can interrupt the communication from a device at the other end and force it to listen. It does this by forcing a low voltage level over the communication line by raising the Control line to a high level. This inhibits data flow over the lines from the slave and causes an error flag in the slave device. As a result, the slave turns into a listen mode (not a hardware feature, but rather incorporated in the software). The slave device can transmit the data after communication from the master device ceases.

The error flag and received data are on the same line. In the listen mode, the Control pin in the master or the TXD (Transmit data) pin in the slave must be held low. Otherwise, the device at the other end can't transmit data over the loop lines.

A 3.3-k variable resistor ($R_1$) is incorporated in the current control path of the loop. This can be used to set the maximum loop current anywhere between 4 and 20 mA. $R_2$ is used for circuit safety and will prevent the loop current from going higher than 20 mA.☐



**AN** error-check mechanism introduced into master and slave communication devices can indicate mismatches when both the master and slave start sending data simultaneously.

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Submissions to the Ideas for Design section should be about one typewritten page of text, with one or two circuit diagrams or block diagrams. They should represent the author's original work, be tested to prove they actually work, and not have been published previously. Please include telephone and fax numbers, if available.

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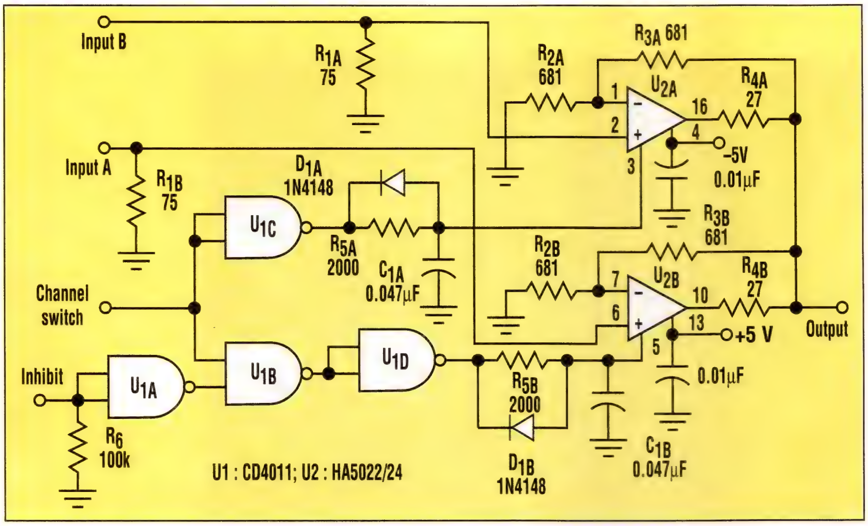
Using op amps that have an enable/disable function, such as the HA5022, will eliminate the multiplexer problems. That's because the external multiplexer chip isn't needed, and the HA5022 can drive low-impedance (large capacitance) loads if a series isolation resistor is employed.

Looking more closely at the circuit, both inputs are terminated in their characteristic impedance; 75 Ω is typical for video applications *(see the figure)*. Because the output cables usually are terminated in their characteristic impedance, the gain is 0.5. Consequently, amplifiers U2A and U2B are configured in a gain of +2 to set the circuit gain at 1. $R_2$ and



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$R_3$ determine the amplifier gain; if a different gain is desired, $R_2$ should be changed according to the equation $G = (1 + R_3/R_2)$. $R_3$ sets the amplifier's frequency response, so it's best to check the manufacturer's data sheet before changing its value.

$R_5$, $C_1$, and D1 make up an asymmetrical charge/discharge time circuit that configures U1 as a break-before-make switch to prevent both amplifiers from being active simultaneously. If this design is extended to more channels, the drive logic must be designed to be break-before-make. Also, the inhibit input is only functional when the channel switch input is high. $R_4$ is enclosed in the feedback loop of the amplifier so that the large open-loop amplifier gain of U2 will present the load with a small closed-loop output impedance while keeping the amplifier stable for all values of load capacitance.

The circuit shown was tested for the full range of capacitor values with no oscillations observed. Thus, the problem is solved. The circuit's frequency and gain characteristics are now those of the amplifier independent of any multiplexing action. This essentially solves the second problem. The multiplexer transition time is approximately 15 $\mu$s with the component values shown.☐

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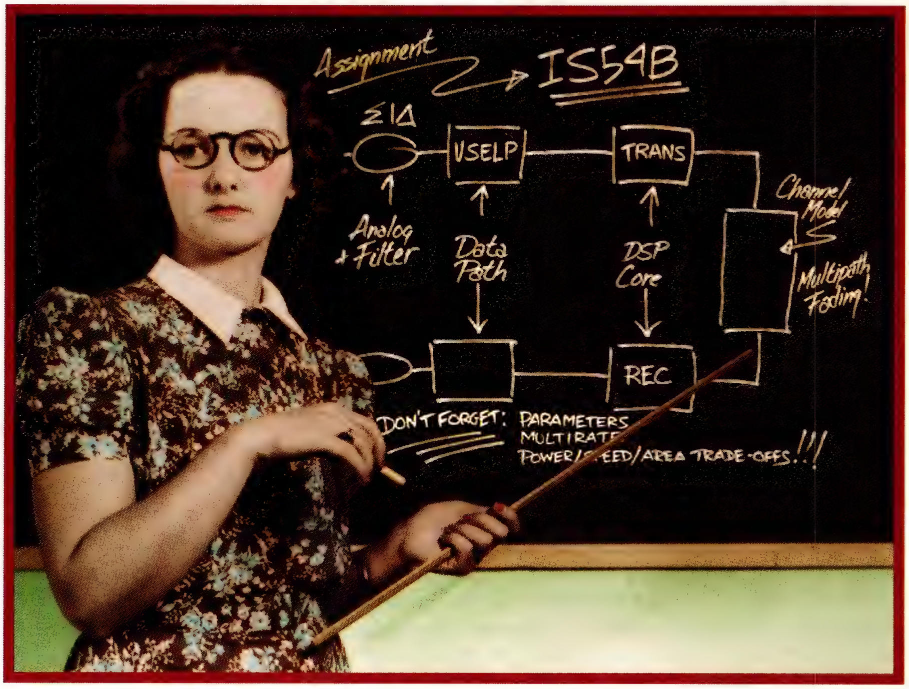

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**READER SERVICE 105**

# ELECTRONIC DESIGN QUICKLOOK

*EDITED BY SHERRIE VAN TYLE*

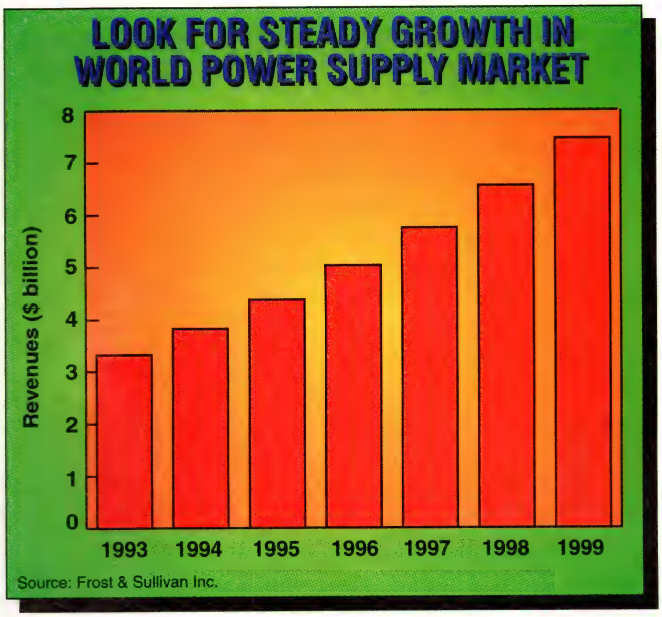
## MARKET FACTS

Thanks to robust growth in computers and telecommunications equipment, the worldwide market for uninterruptible power supplies (UPS) is expected to more than double between 1993 and 1999, increasing from $3.3 billion last year to $7.5 billion by 1999. That's according to Frost & Sullivan Inc., Mountain View, Calif., market researchers.

Innovations in power supplies include power conditioning, systems that can shut down unattended program operations in case of blackout, onscreen display of the time remaining for saving data, and switches to backup systems in less than 5 ms. Responding to demand from data processing and telecommunication industries, makers of UPS equipment are making the units more reliable and less noisy.

Besides computers and telecom, UPSs are being pressed into service in medical applications, instrumentation, utilities, the petrochemical industry, and other heavy industries. Vendors are also looking to the worldwide market, in particular Eastern Europe. For their part, makers of power supplies in Taiwan and South Korea are producing units at highly competitive costs. Lack of an international standard increases manufacturing costs overall, however.

LOOK FOR STEADY GROWTH IN WORLD POWER SUPPLY MARKET



Source: Frost & Sullivan Inc.

## EYE ON ISO 9000

The Datron Div. of Wavetek Corp., a supplier of calibration instruments, has received ISO 9000 certification. For information, contact Patsy Campbell, Wavetek Corp., 9145 Balboa Ave., San Diego, CA 92123; (619) 279-2200. *BN*

CIRCLE 460

IBM's Microelectronics Div. has been awarded ISO 9001 for its East Fishkill-based ceramic packaging business, which develops, designs, and manufactures high-reliability interconnection solutions, from cost/performance products to high-performance products. For information, contact IBM Microelectronics, Media Relations, 1580 Route 52, Internal Zip B, Hopewell Junction, NY 12533-6531; (914) 894-8055. *BN* CIRCLE 461

Keithley MetraByte one of the world's largest suppliers of PC-based data acquisition hardware and software has received ISO 9001. For more information, contact Keithley MetraByte, 440 Myles Standish Blvd., Taunton, MA 02780; (800) 348-0033; fax (508) 880-0179. *BN* CIRCLE 462

Sharp Microelectronics Technology Inc., which develops and produces LCD technology products, camcorders, microwave ovens, electronic organizers, copiers, facsimile machines, calculators, and electronic components, has received ISO 9002. Contact Sharp Electronics Corp., Microelectronics Group, 5700 N.W. Pacific Rim Blvd. No. 20, Camas, WA 98607; (206) 834-2500; fax-8903. *BN* CIRCLE 463

GFS Manufacturing, the only custom magnetics manufacturer on the East Coast to receive ISO 9001, produces transformers and inductors. For further information, contact Janet Sylvester, president, GFS Manufacturing, Inc., 140 Crosby Rd., Dover, NH 03820-4371; (603) 742-4375. *BN*

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Micron Semiconductor Inc., a subsidiary of Micron Technology Inc., a manufacturer of DRAMs, fast SRAMs, and other semiconductor products, has been certified to ISO 9001. Contact Micron Semiconductor Inc., 2805 East Columbia Road, Boise, Idaho 83706-9698; (208) 368-4000; fax -2536. *BN* CIRCLE 465

Chatham Components Inc. has received ISO 9001 for its nine different models of thermal cutoffs in both axial and radial configurations. For more information contact, Dick Perst, Chatham Components Inc., 33 River Rd., Chatham, NJ 07928; (201) 635-8075; fax -6345. *BN* CIRCLE 466

Varian Canada Microwave Products, a subsidiary of Varian Associates, Inc., a leading supplier of power supplies, klystrons, traveling wave tubes, and millimeter wave tubes for communications, radar, medical diagnostic, X-ray, and industrial markets, has been awarded ISO 9001. Contact Varian Associates, Inc., 3050 Hansen Way, Palo Alto, CA 94304-1000; (415) 424-3881. *BN* CIRCLE 467

## OFFERS YOU CAN'T REFUSE

A free design estimator demo for users of PAL/TTL and EPLDs from Xilinx Inc. shows how the company's erasable programmable logic designs integrate multiple PALs, TTLs, or EPLDs while using less board space and consuming less power. It also acts as an interactive teaching tool for the software benefits of the company's EPLDs. The demo, which runs on PCs and compatibles, prompts users to enter new or existing design specifications with the help of a "pop-up" menu that lists all PALs, TTLs, and competitive EPLDs. It then estimates the number and type of Xilinx EPLDs needed to replace the PAL, TTL, or EPLD-based design. The user receives a faxable print-out with the optimal solution highlighted. The print-out can be faxed to Xilinx. Contact Xilinx Inc., 2100 Logic Dr., San Jose, CA 95124; (408) 559-7778; fax -7114.

CIRCLE 468

The fifth edition of the PC/104 Consortium's Resource Guide is free to engineers developing embedded systems. The PC/104 standard, the basis of a new IEEE draft standard (P996.1), defines a compact, self-stacking, modular form-factor for embedded IBM PC and PC AT-compatible system functions within embedded microcomputer applications. The 140-page guide includes an overview of the PC/104 standard, a cross-reference of PC/104-related products and functions, and product listings from the consortium's member companies. For the guide or for more information, contact the PC/104 Consortium, 809 B-175 Cuesta Dr., Mountain View, CA 94040; (415) 903-8304; fax (415) 967-0995.

CIRCLE 469

A cost-analysis disk is free from Creative Forming Inc.'s Electronic Packaging group. With the disk, designers can compare a company's present packaging system against a system incorporating thermoformed packaging components. Included in the analysis are the labor, material, and freight savings that could be realized with a thermoformed packaging system. The user enters the data; then the program calculates and prints a side-by-side comparison of the potential total annual cost savings. Available on a 3.5-in. disk, the program runs on IBM PCs and compatibles. For more information or the free disk, contact Creative Forming, P. O. Box 128, Ripon, WI 54971-0128; (414) 748-7285; fax -9466.

CIRCLE 470

## KMET'S KORNER

# ...Perspectives on Time-to-Market

**BY RON KMETOVICZ**
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

Sometimes I assume too much, but then a whack on the head wakes me up—thank goodness. The latest blow took place at the Custom Integrated Circuit Conference, CICC, held in San Diego. I participated in a panel discussion formed to address reducing new product development cycle time. In preparation, our session's moderator hosted an introduction and discussion dinner. Here, I learned that some of you contemplate reducing your cycle time by a factor of 10. Whack!

What does this mean? Some panel members thought it meant that you take the average of what you do now and divide it by ten to set the goal. Using this method, a current 18-month cycle time becomes 1.8 months. Another panel member viewed the 10-times reduction another way. To set the goal, count the number of products your organization introduced in the past five years. The goal for the next five years becomes ten times the number of products introduced in the previous period.

Numerically, 10 products introduced in the past becomes 100 products in the future. Another view suggests that maybe people may express the view of reducing cycle time, but they do not really mean it—after all, it is only a long-term goal that is not measurable in the short term. Is it possible that these, or a modification of these views are present in your organization? Do you have to deal with this issue?

Varying interpretations of time interval measurement also presented themselves. One view suggested that the measurement of cycle time should not start until thorough simulations, or prototyping, of the intended salable product is completed. Or some suggested starting the measurement of the cycle time interval when their organization actually staffed the project. Others thought the starting point coincides with the first internal presentation of the product idea.

Thoughts on the end point of the interval also varied. One group marked the end at the point of first customer shipment; others supported the measurement of interval completion when volume manufacturing materialized. Where do you stand?

Along with reviewing the goal's fuzziness, our small group questioned the reasonableness of the goal. What would new product development be like if you actually achieved it? Could an organization handle a full order of magnitude increase in product output? Could the customer?

Views on this topic had a central theme. If products served an existing market, the customer controlled the rate of product introductions, not the product development organization—if your customers now go as fast as they can, expect a revolt when rapidly dumping change upon them.

On the other hand, your customers expect you to make improvements and welcome them when presented at a comfortable pace. So improved performance, assuming that the 10-times goal realization has little impact on existing markets, gives you the freedom to take your output windfall and apply it to the creation of new markets. Because you have all this speedy capacity, you bang out in new directions. The days of market sharpshooting become a thing of the past—load those shotguns folks!

I've raised some issues with this column. Discussions, recommendations, and possible solutions follow . . .

*Ron Kmetovicz's The One-Minute Time to Market Self Assessment, which identifies five key behavioral patterns exhibited by fast-moving new product development organizations, is available free to the readers of Electronic Design by contacting Time to Market at the address above.*

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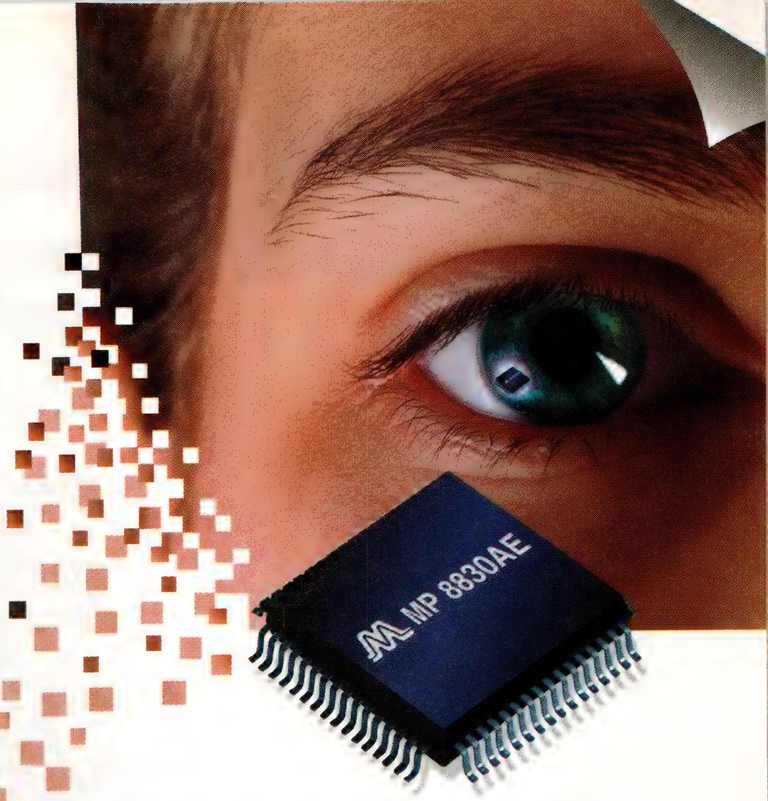

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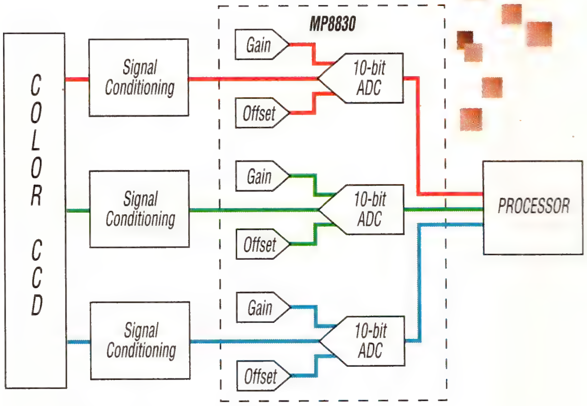

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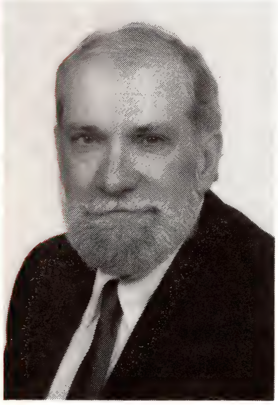
READER SERVICE 163

MY VIEW

# ...Customers know better

### BY FRANK J. BURGE

Director of Market Development for Electronic Design



Twenty years ago I quit doing business with my favorite hotel in Southern California because it had started to go downhill. Staying there just wasn't worth the hassle. Recently I was in the neighborhood and when I drove past the hotel, it looked as if had been spruced up—freshly painted with pretty flowers and shrubs planted out front. I decided to stop and go into the lobby, which had been tastefully renovated. There was a beautiful garden out back. This may explain why the sign out front now reads "Garden Hotel."

I figured that the next time I was in Southern California overnight I'd stay there, for old times' sake. Three weeks ago I checked into the "Garden Hotel," figuring it would be pleasant to stay there. When I arrived at my room, it had an offensive odor so I asked for a different room. No problem, except as I would find out later, the air-conditioning system was on the fritz, so it was very warm in the room all night.

The next morning I got up early to make some phone calls only to discover that the hotel's long distance service was inoperable. When I called the front desk, it was suggested that I use the phones in the lobby. Having given up on the phone caper, I decided to take a shower, which was like turning on a high pressure fire hose, without a way to adjust the nozzle. The accordion-like shower door wouldn't close so there was an inch of water on the floor when I got out. Then as I was dressing, the fire alarm went off because of a malfunction. Nutso.

I met two business associates for breakfast in the hotel coffee shop and it took about ten minutes to find the waiter. After he took our order, he went on vacation. One friend was on a tight schedule so he had to leave before his order was delivered, but he did manage to drink a half cup of cold coffee. Obviously, I will never do business with the Garden Hotel again.

My hotel experience reminds me of what is happening in some companies today. The company loses market share, and the bottom line begins to give Wall Street the willies. So management decides to take action, spruce the place up, and reengineer the organization. Consultants are brought in to apply a few coats of paint and plant a beautiful garden, creating all the appearances of a company on the move. Jobs are cut, and the bottom line recovers on the backs of thousands of employees who are tossed in the dumper. The garden is beginning to bloom and what a sight it is. But the Wall Street crowd remains skeptical. While the bottom line looks good, the top line remains flat, even sinks a bit. And before long, the company hits the downsizing wall and begins to cut into its ability to compete. The top line spirals down, out of control.

Of course, it takes more than a few coats of paint and a freshly planted garden to win customers. For starters, it means listening to the customer, understanding where the customer is today and where he is going tomorrow. And it means helping the customer not only understand where your company is today but where it will be tomorrow. Sharing your technology roadmap with the customer is difficult for some. What if the competition finds out where you're going and beats you there? Chances are your competitors don't care where you're going—they only care about what they have to do to align their offerings with the customer's present and future needs. Some companies still don't get it—they don't get the need to have open communications with customers. It takes more than a beautiful garden.

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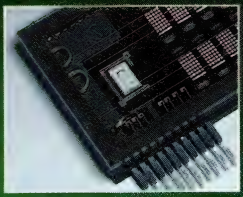

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| FC20X1SA-AB | 20 x 1 | 9.0 x 6.3 | 26.5 x 230 x 23 |
| FC20X2JA-AB | 20 x 2 | 5.05 x 3.35 | 34 x 161 x 23 |
| FC40X1LA-AB | 40 x 1 | 5.0 x 3.3 | 26 x 256 x 23 |
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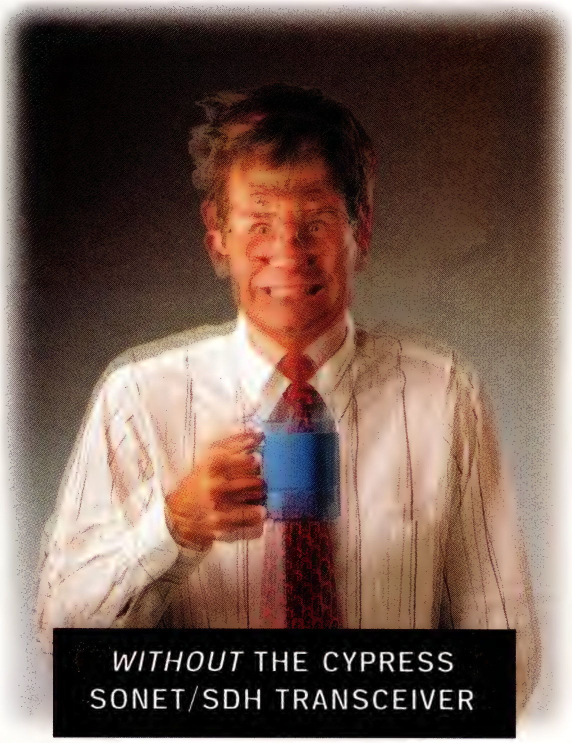
READER SERVICE 117

# DELICIOUS ATM, WITHOUT THE JITTERS.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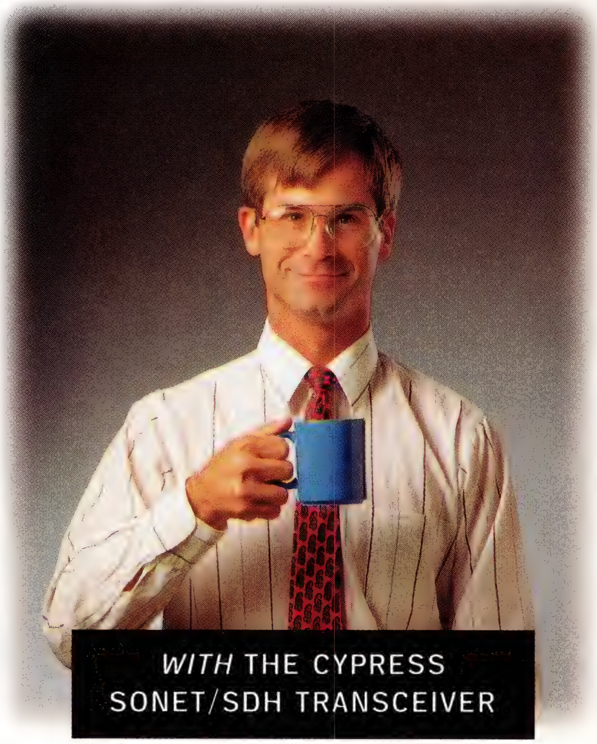
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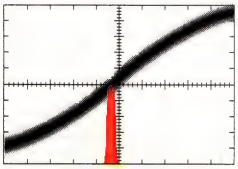
Here's a wake-up call for anyone designing-in ATM functionality: the CY7B951 SST™ (SONET Serial Transceiver) clock recovery chip from Cypress. With its miniscule jitter of just 10 ps, the SST is as close as you can get to guaranteed flawless performance in your ATM environment.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In fact, it is the only solution to support both major ATM application frequencies (51.8 OC-1 and 155.52 MHz OC-3.)

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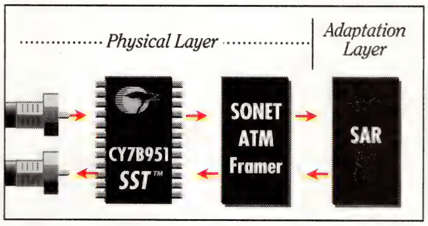

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CYPRESS

# PEASE PORRIDGE

## What's All This V-F Converter Stuff, Anyhow? (Part II)

*If you have already read Jim Williams' compilation, "Analog Circuit Design: Art, Science, and Personalities,"*[1] *then you may look on this column as a summer rerun. However, several people, after reading my 1993 comments on Frequency-to-Voltage converters, asked my opinions on Voltage-to-Frequency Converters. I realized I had written all this down already, so here is a serialized version of the chapter I wrote in Jim's book—reprinted with the kind permission of Butterworth-Heinemann, Boston, Mass. Meanwhile, I'm going hiking.—RAP*

**BOB PEASE**
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

In my June 27 column, I promised to tell you all about the development of the 4701 V-to-F Converter, so here's the story. Refer to the figure for the schematic. I realized that my original circuit had depended on the power-supply magnitude for its Gain Factor. So, it had no power supply rejection, or, to be more nearly correct, it had a PSRR of about 0 dB. So I added a Zener in a bridge to create a PSRR of perhaps 45 dB. (Note, that was the first time I had ever seen such a Zener bridge—was I one of the earliest inventors of that circuit? It's a *neat* and useful circuit.) I also added improved features around the amplifier itself to improve the startup and the accuracy. I replaced the (sole-sourced) 805BE with the more popular and inexpensive LM301A.

I gave the breadboard to my technician, Dick Robie, to oven it and graph out the tempco from the temperature data. That night, when I was on the way out the door, I stopped and asked Dick what had he seen for the tempco. He replied, about zero. I asked, "Whaddya mean, zero. You mean, down near 100 parts per million per degree C?" He replied, "Oh, much better than 100—less than 10 ppm per degree C."

I was shocked. How could it be that good?? The next day, I figured out the fortuitous situation: For the "charge-dispensing capacitor," I had, of course, used one of the best capacitors in the house, the most precise and stable ones, which were polystyrenes with a tempco of –110 ppm/ °C.

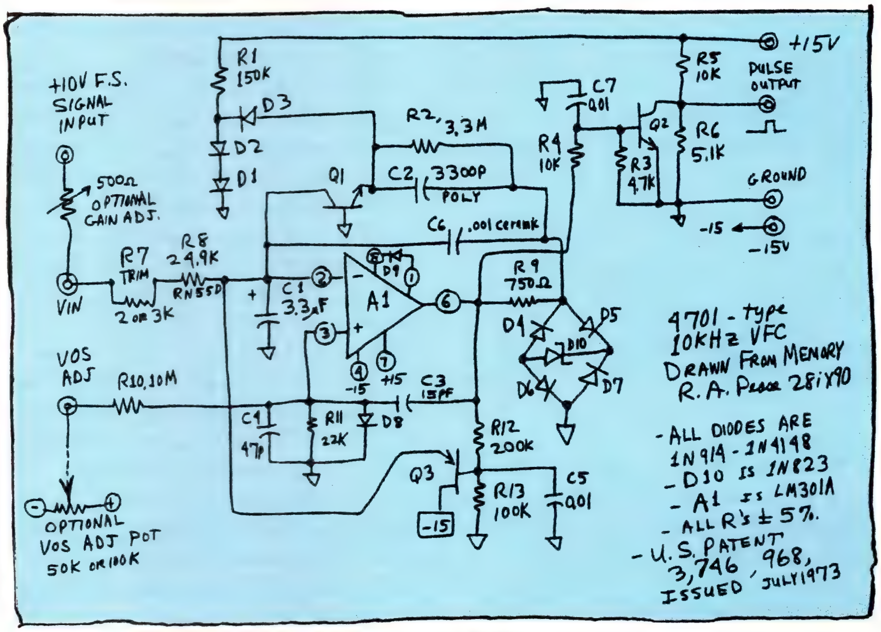
This tempco was just about cancelled out by the tempco of the entire group of diodes in the rest of the circuit. Namely, the driven end of the capacitor moves about 12.4 V p-p, plus the $V_f$ of 4 diodes.

These 4 diodes run rich at about 6 mA, and have a tempco of about –2.0 mV/ °C. The peak-to-peak voltage of these 4 diodes is approximately cancelled by that of the other four $V_{be}$s at the other end of the Polystyrene capacitor, but those diodes run at about 0.1 mA, and their tempco is about –2.3 mV/ °C.

The difference of these is about 4 × 0.3 mV/ °C, or 1.2 mV/ °C, which is about big enough to cancel out the –110 ppm/ °C of the capacitor. Now, there were several things I could have done to fix it if the tempcos hadn't come out even. For example, I could have used 3 diodes, or 5, or 4 1/2, or 3 1/2, but if 4 was the right answer, I'd go with it.

Now, how DOES this Kluge Work?? The best way for me to explain how the 4701 V-to-F Converter really works is for you to trust me, and assume that it *really does* work. After we analyze each section of it, then you will agree that was a reasonable assumption.

First, let's assume that the – input of op amp A1 is a few millivolts more negative than the + input, and that $V_{in}$ is some positive voltage. Rather



soon, the voltage at the – input will cross over and exceed that of the + input. Now, during this time, A1's output has been at the + limit, near +13 V. But when the inputs cross, the output will rapidly slew to –13 V. What are the interesting things happening then?

(1) Because there's positive feedback through C3 = 10 pF, the + input is driven a few volts negative. This ensures that there will be a good wide healthy pulse—at least 17 or 21 µs.

(2) The right-hand end of C2 is driven from about +7.5 V to –7.5 V, and the left-hand end of C2 is discharged through the emitter of Q1. That's a specific amount of charge, $Q = C \times \Delta V$. And the ΔV isn't just the 15 V p-p at the right-hand end of C2, but rather it's that 15 V p-p *minus* the 2.5-V p-p excursion at the left-hand end. When this charge is driven into the emitter of Q1, it comes out of the collector (well, at least 99.5% of it does) and pulls the voltage on the 3.3-µF capacitor down by about 12 mV. During this time, the voltage at the + input of A1 is much more negative than that, so this step of –12 mV is just a minor jump. But, that charge is the magic element of precision. You see, the size of the 12-mV jump isn't important, but the amount of *charge* is.

Note, in most conventional V-to-F converters, the charge is dispensed by a timer circuit such as an LM555, which gates a current ON and OFF, so $Q = I \times T$. However, you do need several precision resistors. Even then, though, the timer is subject to drift and noise, making it a rather crude, drifty, noisy, unstable kind of charge dispenser. In the 4701, the gain depends almost entirely on just 3 elements—the Zener voltage, the capacitor, and the input resistor R8. It's true that the diodes enter in, but since the $V_f$s of D1, D2, D3, and Q1 cancel out the $V_f$s of D4, D5, D6, and D7, then there's not a lot of error or drift likely there.

(3) Now that the output is staying at a negative 13 V and most of the charge on C2 has flowed through Q1, there are 2 more details going on:

(a) During this time, the current through R2 pulls at the emitter of Q1 and makes sure that Q1's emitter settles at a stable voltage. It makes sure that Q1's emitter voltage doesn't tail off to some drifty voltage. Even though R2 looks like it will dump in current that would hurt precision, it actually helps the precision. Even though a precision capacitor used in a precision VFC would normally not have a 3-MΩ resistor across it leaking like crazy—this circuit thrives on *exactly* that "leakage"—because it makes the emitter voltage settle to a consistent level.

(b) The voltage at pin 3 of A1 ($V_3$) is tailing up gradually to be more positive than the voltage at pin 2 ($V_2$). After all, pin 2 was pushed down 12 mV. Soon, after about a total of 20 µs, $V_3$ will cross $V_2$ and the output will bang back up to +13 V.

(4) Okay, now finally $V_3$ crosses $V_2$ and A1's output goes positive. We have to wait for the current through R8 to pull $V_2$ up the 12 mV that it was pushed down. That time will, of course, depend (inversely) on the size of the signal input; the bigger, the faster. That means the time between pulses could be anything between 90 µs and 9 or 90 ms.

Are we forgetting something? Yes. The peak-to-peak voltage at the left end of C2 must be stable and constant and invariant of rep rate. But the diodes there might give a long tail—the voltage might settle gradually and give a different peak-to-peak value at different speeds. By definition, that would hurt the linearity.

What's the fix? The current through R2 is the fix. That current flows through D1, D2, and D3, and forces the left end of C2 to settle to within a millivolt or two of its final dc value in just 50 or 60 µs. Without R2, the linearity goes to pot. Now, it looks REALLY STUPID to have a circuit like this in which the "precision capacitor" C2 has a resistor across it that makes so much "leakage." But that controlled "leakage" turns out to be EXACTLY the reason for the precision and excellent linearity. The Swedish design didn't have this, and while their circuit had good linearity at 1 kHz, it couldn't be made to work well at 10 kHz. But the basic charge dispenser, when driven with suitably fast transistors, works well at 100, 1000, and even 5000 kHz.

What else is in the circuit? D8 is needed between pins 1 and 8 of the LM301A to keep it from wasting excessive current in its – limit. D9 works well to protect the + input from overdrive in the + direction. Q3 functions only when you overdrive the input—let's say, pull $V_{in}$ up to +50 V—and put in so much current that the VFC stops. Then it stops with pin 2 of A1 at +1 V, and pin 6 at –13 V. It would never put out another pulse. It would never restart, even if $V_{in}$ falls to a legal level, such as +1 or +5 V. However, we have added Q3. So, after a lag, C5 gets pulled minus, and Q3 turns on and pulls pin 2 so low that operation does start again. In normal operation, Q3 just sits there and does nothing, biased OFF.

C7 acts as a pulse stretcher. The pulse width at the output of A1 is about 22 µs. But we had a companion F-to-V converter, the 4702, that could only accept 20 µs (or wider) pulses. If A1's output pulse got any narrower than 20, the 4702 would lose accuracy. We solved the problem by putting in C7. Therefore, when A1 makes a 20 µs pulse, the base of Q2 would be held off a little longer than that due to the RC lag—about 15 µs extra. Then a 4701's pulse was always plenty wide enough to drive a 4702.

The little capacitor C6 was added to make the peak-to-peak voltage at $V_2$ a little bigger. So, when some LM301's were a little slow, there was now a bigger signal between $V_2$ and $V_3$, and the amplifier wouldn't balk. After all, the LM301 is characterized as an operational amplifier, and if some are a little slower than others when you run them as a comparator, you really can't complain....

As you can see, the 4701 circuit did get a couple of band-aids, but not too many, and we never really did get stumped or stuck in production. Our customers loved the linearity, the tempco was pretty good, and the frequency output would never quit. The customers figured they really got their money's worth, and I certainly couldn't disagree with a satisfied customer.

I got my boss, Dave Ludwig, to ap-

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# PEASE PORRIDGE

prove the layout of a printed-circuit board, and I think Wayne Norwood was the guy who laid it out. We built up a few dozen and evaluated them thoroughly. I wrote up a draft of a data sheet, and I negotiated with Skip Osgood and Bill Bernardi to get it printed properly. I made up some test equipment and we got a silk screen for the module, and we called it the 4701. We were in the Voltage-to-Frequency Converter business.

To this day, I don't recall exactly how we got these V-to-F Converters to be so popular. I can't recall how we found so many customers, or how we publicized the VFCs. I asked Frank Goodenough because I knew he had been involved. He recalled that he had looked at some of the characteristics of this 4701, and he suspected that a good V-to-F Converter might be useful at The Foxboro Company, the big process-control experts. Indeed, he did find some interest there. The company was very interested, but it never bought very many because they wanted to buy only parts available from multiple sources.

The 4701 became popular, with many customers at many companies. It became profitable. It became good business. If I had all the time and space in the world, I would tell you how the 4701 led to the 4702 (a 10-kHz F-to-V Converter using the same charge-dispensing principles) and the 4703 (100-kHz full-scale VFC) and the 4705 and 4707 (1-MHz and 5-MHz VFCs). Also, the 4709, 4711, 4721, and 4715 VFCs, and 4704, 4706, 4708, 4710, and 4722 FVCs. Some of these had a moderate tempco of 150 or 44 ppm/ °C, but some were well-trimmed and guaranteed to 6 ppm/ °C—as good as the best DVMs of the day.

But it all started with that crummy little 4701—and the principle that one cheap operational amplifier driving a little charge dispenser could make a very linear data converter. This came from an understanding that you could build an oscillator with a UJT and an operational amplifier to help improve the linearity, and *then* throw out the UJT!! I was able to do that because I was receptive to the concepts that would make a good Voltage-to-Frequency converter, even though I had never seen a Voltage-to-Frequency converter!

I was able to make accurate measurements, to throw in precision components—Zener references, capacitors, resistors—and to get inexpensive IC amplifiers, and to optimize the whole little system. What's the lesson for us to learn?

I like to think of the words of Branch Rickey, manager of the St. Louis Cardinals in the 1920s (and later manager of the Brooklyn Dodgers). One of his favorite sayings was "Good luck is the residue of design." When he referred to his baseball teams, he meant that his players were able to handle any play, field the ball, throw to the right base, etc., no matter how surprising the bounce of the ball might be.

If his players had learned the fundamentals, if they were prepared for any situation, they could take advantage of game situations and WIN. Other people might say his players were just lucky, but he knew darned well that he had trained them and drilled them so they would instinctively know to do the right thing.

I, too, was in a situation where I was prepared to take advantage of the opportunity, and I didn't drop the ball when it came my way. (Well, I fumbled it for a while but then I got it right.) That's the point of this column: When somebody hands you a gift on a silver platter, you really must be prepared to recognize it.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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References:

1. *"Analog Circuit Design: Art, Science, and Personalities,"* edited by Jim Williams, 1991. 398 pages. Butterworth-Heinemann, Boston, Mass., (800) 366-2665. About $51. An excellent book; you should have your librarian order it.

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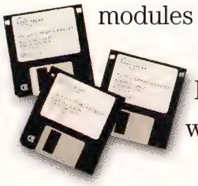

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# COMPUTER SYSTEMS

A SPECIAL EDITORIAL FEATURE

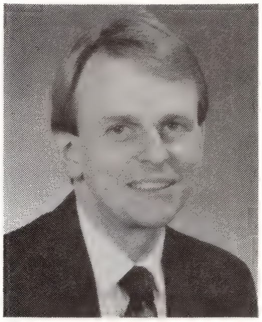
**PC GRAPHICS WATCH**

# USING THE DDC

ANDERS FRISK, ICL PERSONAL SYSTEMS

In 1991, the VESA Monitor Committee established an agreement on what was then thought to be ergonomically adequate CRT monitor timings for 15-inch and smaller displays. However, some manufacturers with an eye on the European markets and those with larger monitors realized that the 1991-vintage 70- and 72-Hz timings wouldn't be sufficient for very long. The committee tried to find a method of giving each manufacturer some way to use the timings that are required for their market segment. They also looked for a way to inform the host computer's graphics controller of the monitor's capabilities at each supported resolution with its corresponding timing. The resulting VESA Display Information Format (VDIF) established a common language to describe monitor capabilities.

Since that time, the PC industry has identified the need for plug-and-play configuration. It became clear that the VESA Monitor Committee had to address the display identification and configuration issue with an open solution that benefits the entire graphics industry. Consequently, the group defined the Display Data Channel (DDC)—a communication channel over which the monitor automatically informs the host system about its capabilities.



The proposal consists of three parts: the hardware interface, the information content, and the BIOS interface. The hardware interface, or DDC level and command set, has two alternatives. The DDC1, a unidirectional communication channel, continuously transfers the EDID information from the display to the host. The DDC2, a bidirectional channel based on the Access.bus, connects low- to medium-speed peripherals to the host system.

A DDC2 device can support either a limited command set (called DDC2B), which just lets the host retrieve information from the display, or the Access.bus command set for monitors (called DDC2AB) in DDC language. The Access.bus Monitor Command Set is currently under joint development by both VESA and the Access.bus Industry Group.

Both DDC1 and DDC2 share the same signal pins in the 15-pin VGA connector. As a result, the DDC can be implemented rapidly in both monitors and host systems. Monitors must support both DDC1 and DDC2, while host systems can support either one. This will assure a complete mix-and-match capability.

DDC is implementable in any monitor simply by adding one memory chip with an integrated DDC interface, a component that's currently being developed by a few vendors. Alternatively, the DDC can be embedded in software in a monitor microcontroller.

In existing designs, applying DDC1 on the host side can be done by adding software that reads EDID data received from pin 12 on the VGA connector. Some designs may need a minor hardware change. Implementing DDC2 requires more significant changes, but is well worth the effort. The benefit is that all types of Access.bus devices can be connected to the host through this interface. If the monitor is Access.bus command-set-capable, the system can perform more advanced monitor control functions through the keyboard and mouse. One difficulty is that the Access.bus-capable host systems must supply +5 V to the host connector. Avoiding improper sequencing of the supply power, which could damage the display and host interface, requires a unique design of the host connector. Socket number nine must be moved back 0.05 in. to ensure proper sequencing. To identify the Access.bus-compatible system and avoid an incorrect connection, the plastic insert in the connector is colored royal blue.

The information content of the proposal, called Extended Display ID (EDID), is a 128-byte block of information about the display. The information is divided into categories: Vendor and Product Identification, in which the data is based on the EISA ID format; and Basic Display Parameters and Features, which holds information about the size, color characteristics, and level of support for the VESA display power-management signaling standard (DPMS). The next three categories define support for various monitor timings. Established Timings is a bit field that indicates support for existing VESA and industry-standard timings; Standard Timings is a field of eight 2-byte identifiers that are assigned once future timings are defined; and Detailed Timings lets the monitor vendor describe (in detail) up to four sets of unique manufacturer timings.

The BIOS interface, called VBE/DDC, is a separate standards proposal describing extensions to the PC video BIOS for retrieving EDID or VDIF information from the display.

*Thanks to Diane Rogers of NEC Technologies Inc., who contributed to this article.*

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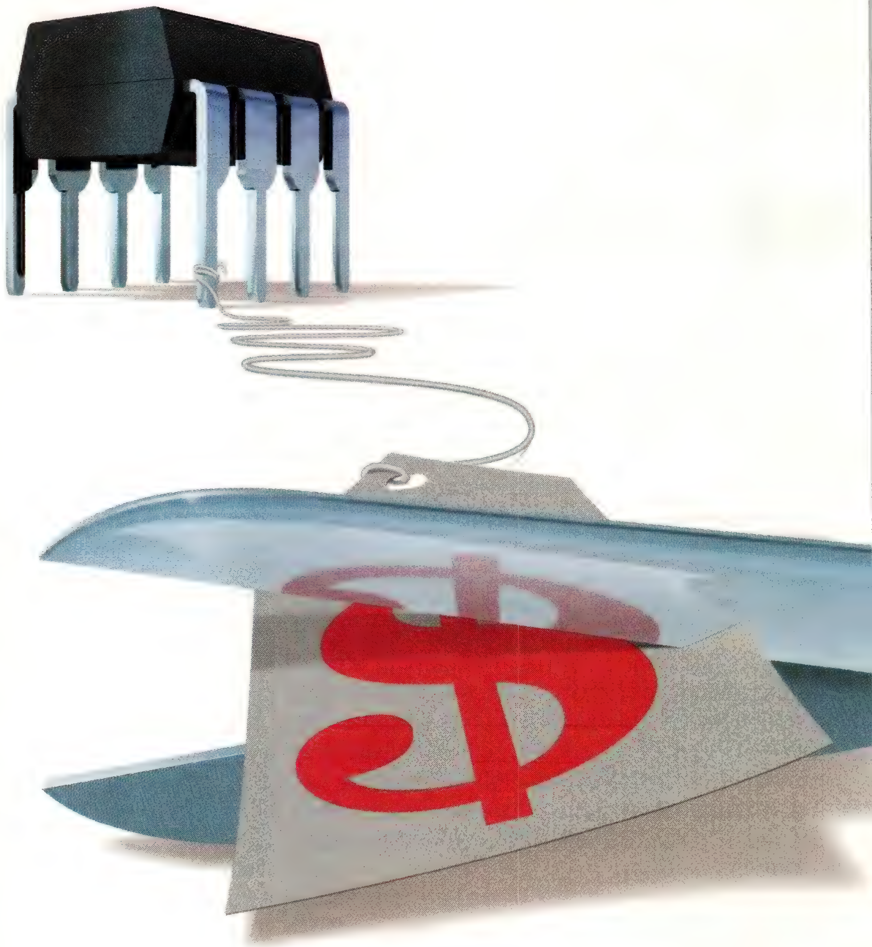

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# Integrate PCMCIA Sockets Into Desktops

### *Adding card sockets to desktop systems introduces new design challenges.*

BY HENRY FUNG

Vadem, 1885 Lundy Ave., #201, San Jose, CA 95131; (408) 943-9301.

PCMCIA card sockets originally were created to solve a specific design problem: To provide a standard interface that expands memory in portable systems. Later, I/O-card expansion was added to the specification. But with the growing range of PCMCIA peripheral and memory cards comes a demand for desktop systems or docking stations that can easily exchange data and share peripherals with portable systems. Today designers are being asked to add PCMCIA card sockets to the desktop. Consequently, those designers face a new set of challenges as they try to adapt what was originally a portable concept to the desktop environment.

Implementing PCMCIA in the desktop requires not only adherence to the PCMCIA standard, but also consideration of several physical and electrical issues. In desktop systems, for example, it's necessary to support both front and rear access for PCMCIA sockets. I/O cards such as LAN adapters require a connection in the rear of the machine, while memory cards, which function like floppy-disk drives, require front access. To satisfy these demands, system designers must consider the complexities of driving signals from the motherboard to the PCMCIA socket through cables. Issues to be resolved include transmission line analysis for the cabling, interrupt sharing to support multiple sockets, and accommodation of the coming Plug and Play (PnP) standard.

In applications where cables connect the cards to the PCMCIA socket controller, the behavior of a given signal traveling from the transmitting point to the receiving point can be affected by the transmission medium as well as its surrounding environment. These phenomena are known as transmission-line effects and crosstalk, respectively. If not handled carefully, they can cause the system to malfunction.

Fortunately, in most cases, designers can solve these problems by following a few rules. For example, the maximum duration of reflection caused by transmission-line effects and noise generated by crosstalk depends on the length and type of insulation used in a particular cable. This duration varies between 3 and 4 ns/ft. of cable. So, for any given logic type, the system can be built with cables up to a specified length without worrying about reflection and noise problems. This holds true because, in general, if a flip-flop input is altered by noise or reflection for less than its setup time, the correct state is still maintained.

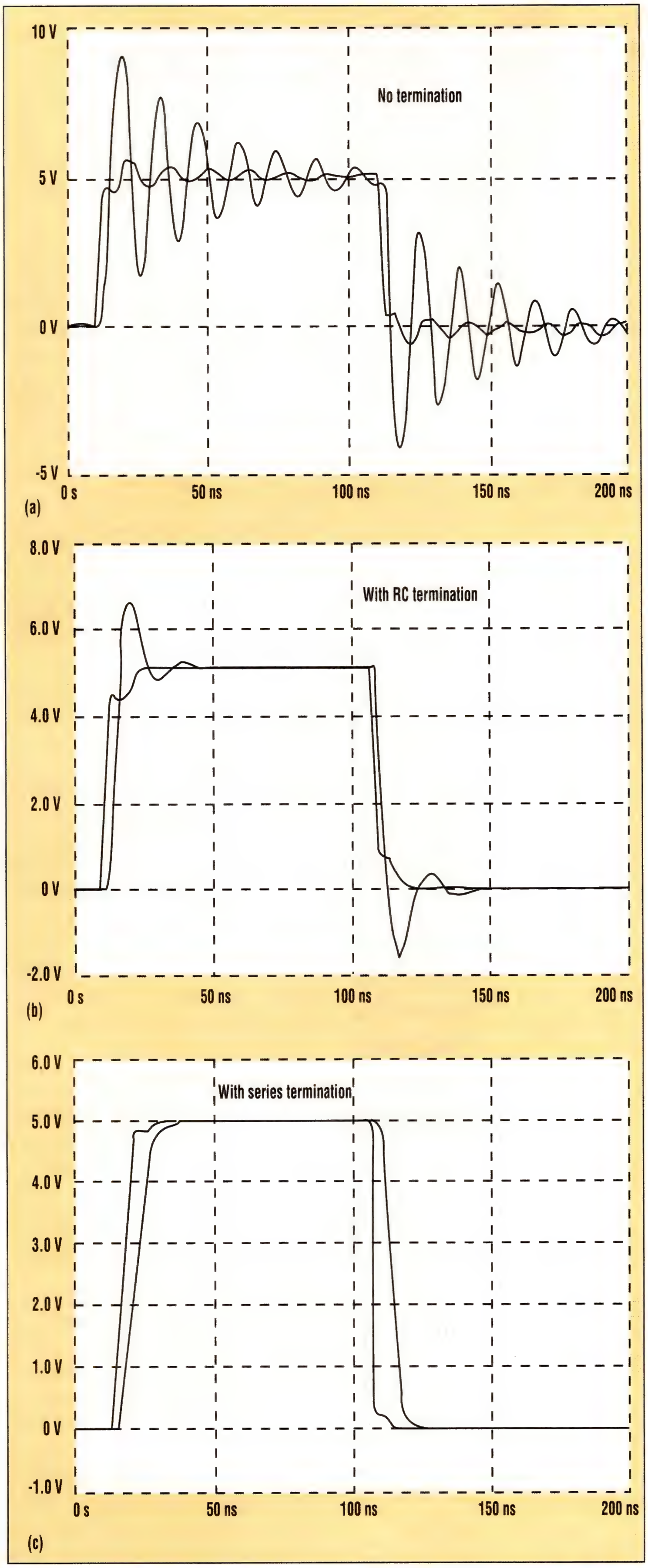
A TTL flip-flop with a minimum setup time of 10 ns, for instance, can be used in a system with cables up to 2.5 ft. (10/4) without adverse implications. If, however, the designer uses fast Schottky TTL flip-flops with minimum setups of less than 2 ns, he will encounter transmission-line problems with cables only 0.5 ft. (2/4) long. High-speed logic circuits can experience problems with cables less than 1 in. Therefore, it's important for designers to limit the logic speed to the maximum speed needed for efficient operation.

The transmission-line concept isn't only useful, but necessary if designers plan to operate a system with cables longer than the maximum lengths calculated for the various logic types. Transmission-line theory states that reflection is produced if the characteristic impedance of a cable connected to the PCMCIA socket controller isn't matched by the termination impedance on the socket side.

**Designers can simulate effects on any given signal and optimize design without actual prototyping.**

With today's CAE tools, designers can simulate the transmission-line effects on any given signal and optimize a design without actual prototyping. The result's accuracy depends greatly on the simulation model and requires the electrical characteristics of the cable, the transmitter, and the receiver. In a model for transmission-line testing, the RC termination removes the dc power load on the system power supply at the expense of increasing the signal edges' transition time. Either RC or series termination can be used in the model.

If the designer chooses to use series termination, the resistor must be located near the socket controller. The transmit and receive waveforms illustrate the transmission-line effects when the system features no termination, RC termination, and series termination, respectively *(Figs. 1a, 1b, and 1c)*. No termination creates a ringing effect, RC termination can generate overshoot and undershoot, and series termination provides a more perfect looking waveform but with some delay. By simulating the system, designers can quickly compare the results of different termination methods and choose the one that best suits the



**1. The plots show the transmission-line effects of a circuit that features no termination (a), RC termination (b), and series termination (c). No termination creates a ringing effect, while RC termination can generate overshoot and undershoot. Series termination offers the best looking waveform, but with some delay.**

application. Other variables required for the simulation include the electrical characteristics of the cable, the transmitter, and the receiver.

One of the major debates in PCMCIA applications is whether buffers are necessary on the socket side. Because PC cards lack some applicable specifications, designers must deduce a number of critical parameters necessary for a worst-case analysis from the available information. For example, the rise time and output resistance and current of the card's output drivers are typically unspecified. As previously demonstrated, the transmission-line model also depends on the electrical characteristics of both the transmitter and the receiver. Without such knowledge, designers can't optimize their models. Driving long cables in high-performance, high-reliability systems demands buffers at the PC-card end of the cable and PCMCIA socket controllers that can control the direction of the external remote buffers. In low-end applications, designers must trade off reliability against lower cost.

Another cabling issue to consider is electromagnetic coupling between signal wires, or crosstalk. In a transmission-line model with coupling from an adjacent signal wire, $V_3$ is always 0 V, $R_{13}$ equals the source resistance $R_1$, $R_{11}/C_5$ equals $R_7/C_1$, and $R_{12}/C_6$ equals $R_2/C_2$. The goal is to induce an output voltage on the neighboring output line (between nodes 4 and 10 on the circuit), due to the fluctuations of the primary line (between nodes 3 and 4) *(Fig. 2)*.

Crosstalk will result on the neighboring signal if the disturbing signal isn't terminated properly, while a well-terminated signal can limit crosstalk to signal transitions. As long as a reasonable clock speed is employed, the signals will have time to settle until they reach the correct final value before the next clock, despite the temporary incorrect

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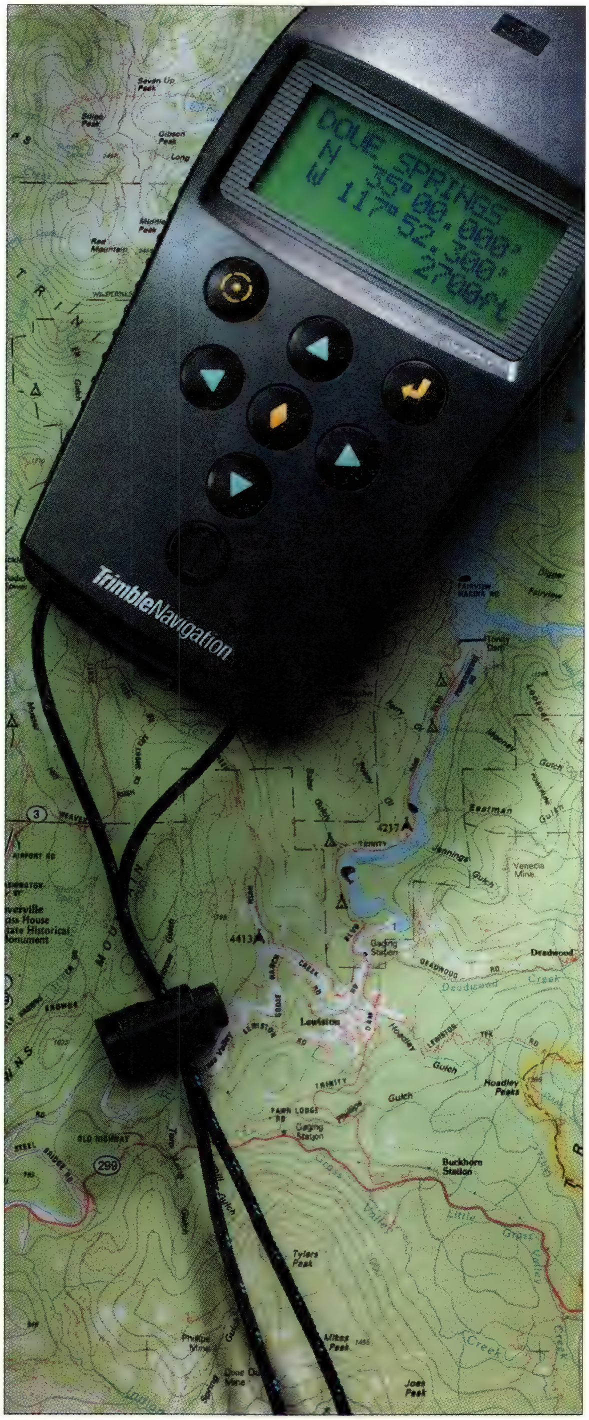

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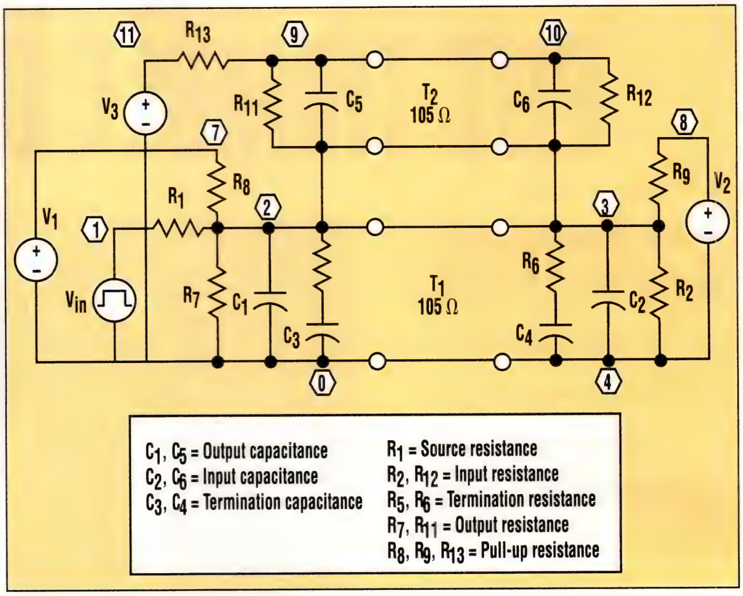
value caused by crosstalk. As a result, crosstalk can be ignored on the signal lines.

One exception to the described scenario is crosstalk back to previous logic levels on ECL systems. This type of crosstalk can cause oscillations due to the formation of positive feedback loops. When TTL is employed, this is less likely to occur, because little time is spent in the transition region where forward gain exists.

One simple way to reduce crosstalk is to use a multilayer pc board with a ground plane. The ground plane lowers the impedance of the individual conductors and partially intercepts the electrostatic (capacitive) and electromagnetic (inductive) fields linking the two conductors. The crosstalk voltage produced on a passive line essentially results from a mutual impedance coming from the disturbing signal lines. This produces a voltage across the line's characteristic impedance (to ground). Therefore, the signal line should have the lowest characteristic impedance and the highest mutual impedance to the disturbing signal. When the distance to the ground plane is comparable to the distance between signal lines, crosstalk rapidly decreases.

Although a multilayer board with a ground plane reduces crosstalk problems, a less expensive, double-sided board with a careful layout often can perform acceptably. Various PCMCIA socket-controller suppliers offer socket-adapter manufacturing kits that employ double-sided pc boards for low-cost production.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10
V3
R11
C5
T2
105 Ω
C6
R12
7
8
R8
R9
V2
R1
2
3
V1
1
R6
Vin
R7
C1
T1
105 Ω
C2
R2
C3
C4
0
4
C1, C5 = Output capacitance
C2, C6 = Input capacitance
C3, C4 = Termination capacitance
R1 = Source resistance
R2, R12 = Input resistance
R5, R6 = Termination resistance
R7, R11 = Output resistance
R8, R9, R13 = Pull-up resistance

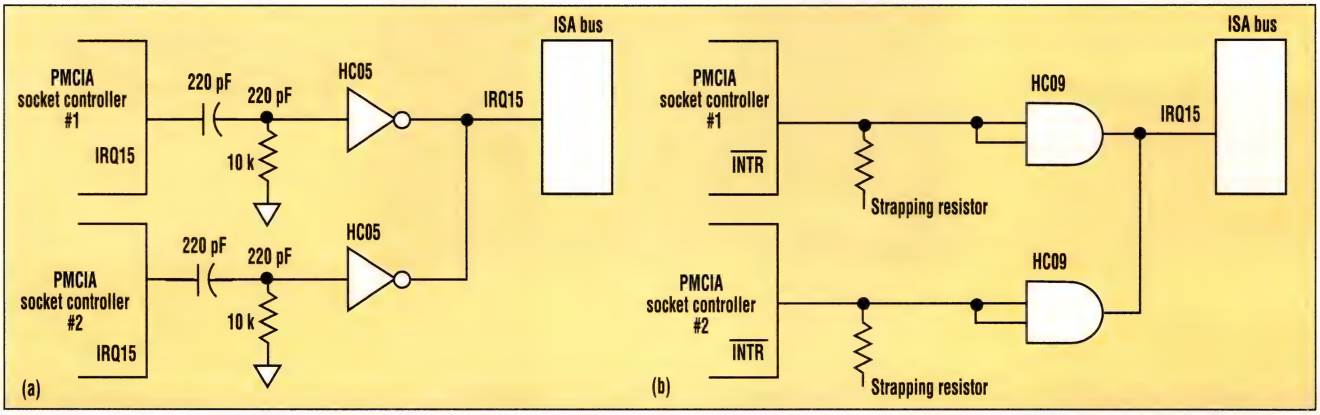
**2. The crosstalk in cables occurs when proper termination isn't present. In the model, the goal is to induce an output voltage on the neighboring output line (between nodes 4 and 10), due to the fluctuations of the primary line (between nodes 3 and 4).**

To further minimize crosstalk, designers can isolate similar buses by surrounding them with ground wires in the flat cable. For example, the array of wires for the data and address buses should each be bordered by two ground wires, and all other control lines should be separated by alternating ground wires in the cable.

While today's notebook computers typically feature a maximum of two PCMCIA sockets, desktop environments frequently require more than two sockets. That presents new addressing and interrupt-sharing problems. The portable's dual sockets are usually supported by a single integrated PCMCIA socket controller. Multiple socket controllers within a system must provide selectable addressing or indexing. It's important to note that not all PCMCIA socket controllers offer the same capabilities in this area. Many controllers support alternative addressing or indexing by either resistor strapping or external decoding. Resistor strapping is relatively inexpensive, but can limit the maximum number of controllers to four (or eight sockets). External decoding allows more flexible addressing, but requires additional hardware. System designers must choose a socket controller that can provide the appropriate capability for their application.

Another problem designers confront when supporting multiple controllers is interrupt sharing. In most designs, the

**3. Here are two ways to handle interrupt sharing with multiple controllers. First, an RC circuit generates a pulse on the IRQ's rising edge, which is inverted by an open-collector 74HC05 inverter, driving the IRQ 15 line on the bus. The pulse's trailing edge triggers the interrupt (a). The second technique uses the $\overline{\text{INTR}}$ signal instead of IRQ 15 for the status change interrupt. $\overline{\text{INTR}}$ is connected to a 74HC09 open-collector AND gate, which drives the IRQ 15 line on the ISA bus (b).**



PCMCIA status-change interrupt usually appears on interrupt-request line (IRQ) 15. PCMCIA socket controllers that only support level interrupts won't be able operate a sharing scheme because the ISA bus requires a low-to-high transition on IRQ 15 to recognize the interrupt.

Here are two example solutions to this problem. First, an RC circuit generates a pulse on the rising edge of the IRQ, which is inverted by an open-collector 74HC05 inverter. It then drives the IRQ 15 line on the bus. The trailing edge of the pulse triggers the interrupt *(Fig. 3a)*. The second technique requires that the Socket Services software be modified to use $\overline{\text{INTR}}$ instead of IRQ 15 for the status change interrupt. $\overline{\text{INTR}}$ is then connected to a 74HC09 open-collector AND gate, which in turn drives the IRQ 15 line on the ISA bus *(Fig. 3b)*. The $\overline{\text{INTR}}$ output is a low-going pulse, and the interrupt is triggered on the trailing edge.

Some PCMCIA socket controllers, such as Vadem's VG-469, don't require external logic to support a shared interrupt. They can be wire-ORed together to form one IRQ 15 interrupt. When the internal STATIRQ-SHARE bit is set, the IRQ that's programmed to be the status change output is normally three-stated, but it pulses low for a few clock cycles when a status change occurs. The pulse's rising edge triggers the interrupt. This satisfies several conditions of the XT or AT system's 8259 interrupt controller when operating in the edge sensitive mode, such as:

1. The interrupt must cause a positive transition edge on the IRQ 15 signal to request the interrupt.
2. The IRQ 15 signal must be in the high state when the interrupt is acknowledged by the CPU.
3. The IRQ 15 signal has a pull-up resistor that causes the signal to remain in the asserted condition when the IRQ 15 signal isn't being driven.

PnP, which makes the installation of add-in cards transparent to end users, will be supported in the upcoming Windows revision. Dynamic system configuration for a notebook computer is never a problem because it's a closed system except when connected to a docking station. And PCMCIA, designed with a form of plug-and-play in mind, supports hot swapping.

The move to "hot docking," however, completely changes the system design. In this environment, resources can be added or deleted from the system at any time. For these systems to run properly, the operating system must maintain complete control of the system resources at all times. But older ISA add-in cards don't give that control to the operating system. Many times, the resources taken by these cards are set by jumper settings and can't be easily reset. The PnP specification solves this problem by defining a set of configuration ports that all PnP-compliant ISA cards adhere to. When requested, the cards will issue their identifications, called the device IDs. And a collision-detection protocol prevents cards from interfering with each other.

Once all of the cards are identified, the operating system uses device IDs to access the correct device drivers and other resource requirements for each card. To comply with the specification, some PCMCIA Socket Controllers provide an interface to serial EEPROM to store device IDs and resource requirements.

*Henry Fung, v.p. of engineering at Vadem, holds BSEE and MSEE degrees from San Jose State University, Calif.*

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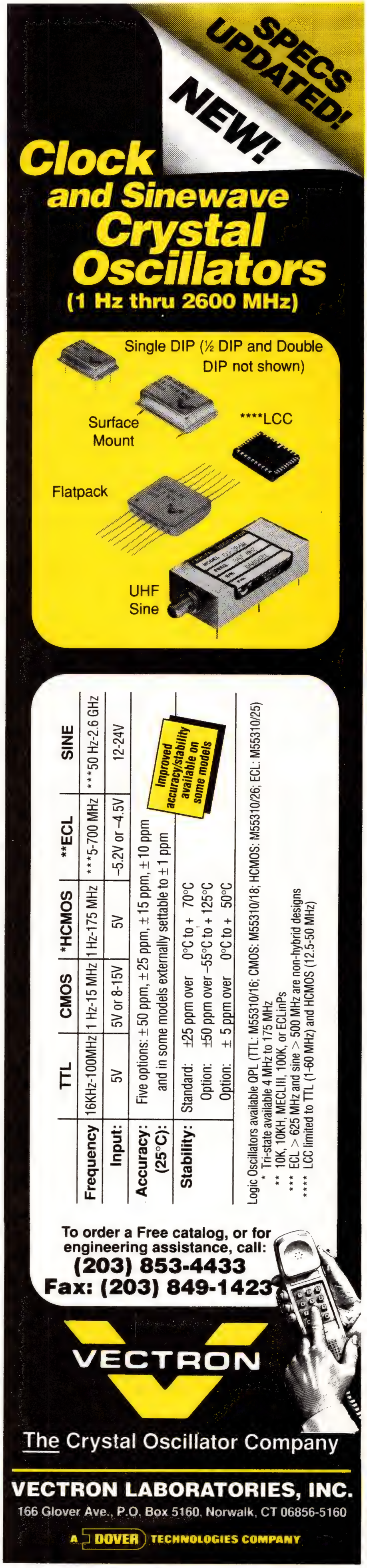
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## SYSTEM DESIGN NEWS

**A new family of gate arrays**, aimed at PCI-based computers, will support 5 V, 3.3 V, and future voltages. The Universal PCI series, developed by NEC Electronics, Mountain View, Calif., also directly drives the peripheral-component interconnect (PCI) bus or Gunning-transceiver logic (GTL). With three supply rails, the arrays can offer 5 V on some I/O lines and 3.3 V on others. As a result, they can be used in mixed-voltage systems and tie in with 5- or 3.3-V PCI buses, or with the universal PCI buffer. In addition, the arrays can handle standard signaling levels for CMOS, low-voltage CMOS, TTL, and LVTTL. Of the 14 arrays in the family, the largest has 223,000 available gates and loaded gate delays of about 290 ps. Typical consumption per gate is 2.7 µW/MHz/gate. The arrays come in 160- to 304-lead PQFPs. NRE charges vary depending on design complexity, but basic packaged chips sell for $6 to $60 each in lots of 10,000. Contact Christina Smith at (415) 965-6000.

**Aimed at 3.3-V desktops or portables**, the Apollo pc chip set includes a PCI bridge interface and enhanced buffering that gives the set a 10% performance gain over competitors. In addition, its integrated power management minimizes power drain during system idling. Created by Via Technologies, Fremont, Calif., the Apollo chips support single and dual 64-bit Pentium 3.3-V CPUs with internal speeds of 100 MHz and higher. They also provide 5-V interfaces for DRAMs as well as for VL, ISA, and PCI buses that can run at up to 66 MHz. The chip set consists of a 208-lead system controller, two 100-pin data buffers, and a 160-lead VLbus-to-PCI-bus bridge. A 100-lead X-bus peripheral controller provides a multi-output clock generator, a real-time clock, keyboard controller, and PS/2-style mouse support. The chip set addresses up to 512 Mbytes of system memory and a second-level cache of 256 kbytes to 2 Mbytes (standard or synchronous SRAMs). Mechanisms are included for shared-memory coherency, burst read/write transactions, interrupt steering, interprocessor communication, and bus arbitration. Samples are available; in OEM quantities the chip set sells for about $48. Contact Dick Renne at (510) 683-3300.

**A family of 16-Mbit synchronous 3.3-V DRAMs** helps meet the needs of high-performance systems thanks to its ability to stream data at 100 MHz. The dual-bank, pulsed-RAS design conceived by Samsung Semiconductor, San Jose, Calif., includes three versions: the KM44S4020A (two banks of 2 Mwords by 4 bits), the KM48S2020A (two banks of 1 Mword by 8 bits), and the KM416S1020 (two banks of 512 kwords by 16 bits). The DRAMs are totally synchronous, with all inputs sampled and all outputs valid at the positive-going edge of the system clock. They require only the starting address and a burst length of 2, 4, or 8 bits. Once the burst begins, valid data is put on the bus every clock cycle. When the burst ends, the outputs are placed in a high-impedance mode. Bursts can be programmed either by incrementing with a linear binary count, or by using Intel's interleave count. Both the 4-bit- and 8-bit-wide units are now sampling; the 16-bit DRAM will be sampled by year's end. All will be available in 77-, 83-, and 100-MHz versions, and initially will cost about 30% more than comparably-sized asynchronous DRAMs. Call (408) 954-7000.

**With a peak bandwidth of 80 Mbytes**, the single-chip MC92005 SBus slave controller offered by Motorola Inc., Chandler, Ariz., operates from 16.67 to 25 MHz. It supports processor clocks up to 60 MHz. Designed jointly by Motorola and Sun Microsystems, the CMOS chip interfaces up to six 32-bit slave devices to the SBus without any other chips. Thanks to a programmable private bus interface (PBus), the SBus configuration PROM and several peripheral devices or memory chips also can be directly connected to the SBus. A prototype board containing the chip and support hardware is available from Dawn VME Products, Fremont, Calif. The MC92005 comes in a 160-lead PQFP and sells for under $30 each in lots of 1000. Contact Gordon McDonald at (602) 814-4560.

### ▼ AUDIO BOARD RUNS DSP OS

A task-managing DSP operating system is embedded into the 16-bit SoundWave 32+SCSI wave-table audio card. As a result, users can change the personality of the card without leaving the Windows operating environment. Different DSP algorithms can be performed in real time, such as 10:1 audio compression, special effects, Q-sound, voice recognition, and music synthesis. Most standard audio formats are supported, including SoundBlaster, AdLib, Windows Sound System, and the Roland MPU-401 MIDI interface and MT-32 sound module.

The board comes with 2 Mbytes of sound samples, while 16-bit stereo audio and ADPCM compression let users record sounds directly to the PC's hard-disk drive. A second wave-table synthesizer can be added for improved sound quality and higher polyphony (up to 56 voices). A CD-ROM interface controller permits connection to SCSI-based drives. Recorder and voice-recognition software comes bundled with the board. The SoundWave 32+SCSI is priced at $279.

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### ▼ TRACKBALL DOUBLES AS PRESENTATION DEVICE

The TrackMan Voyager, which is a trackball that works with both desktop and portable computers, can be used as a handheld presentation device. The device's small form factor and integrated cover make it easy to carry and comfortable to use. It can be operated in five different positions. The enhanced driver software lets portable users adjust the cursor speed and directional orientation of the trackball and also set the three buttons for customized functions. Common commands such as double clicking can be assigned to one click for higher efficiency. The TrackMan Voyager is available now for $89.95.

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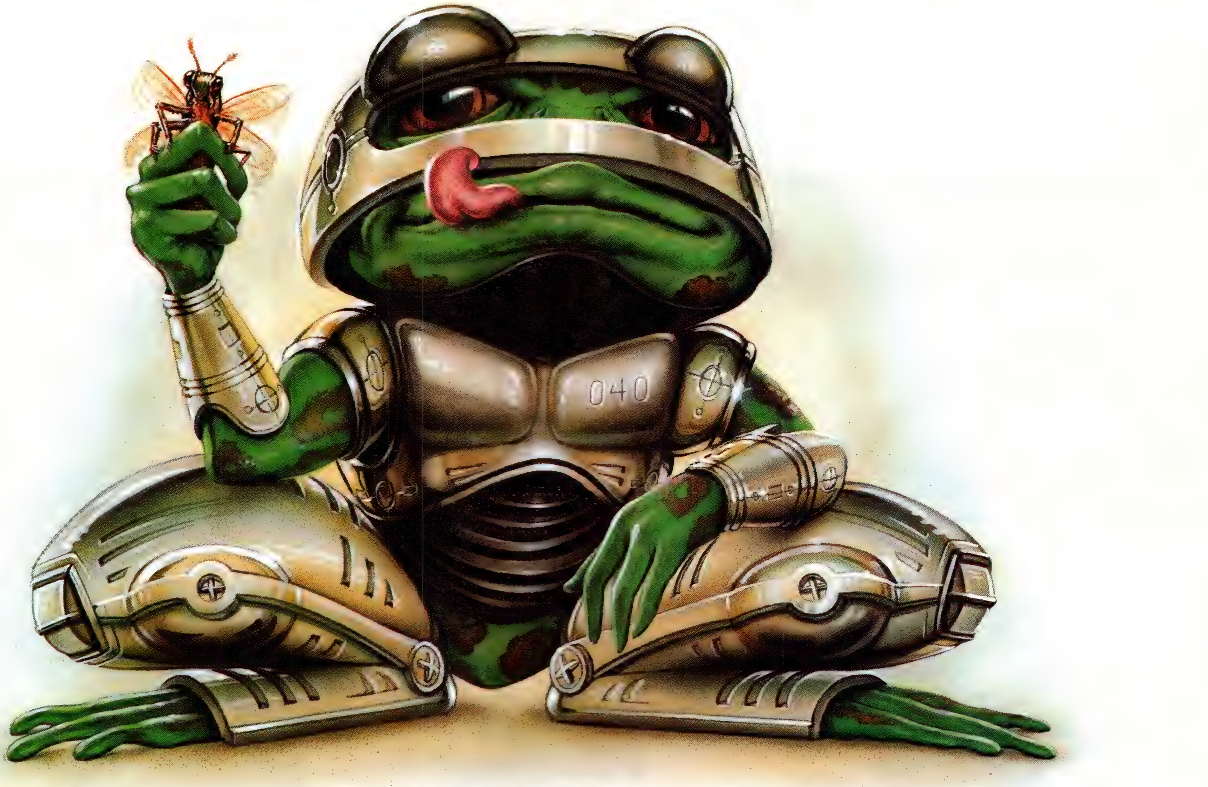

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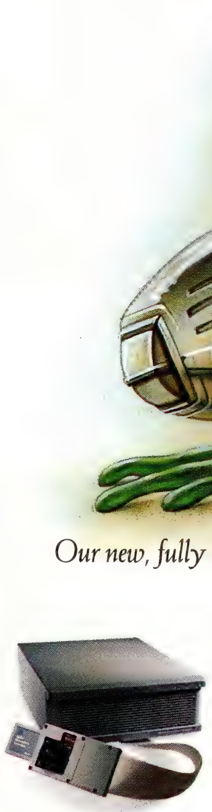

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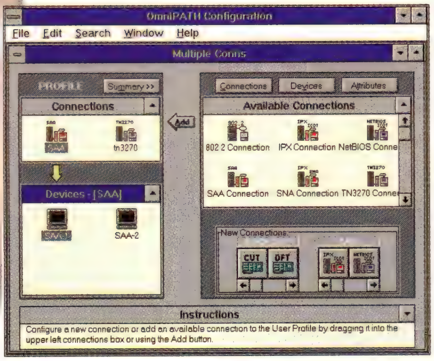

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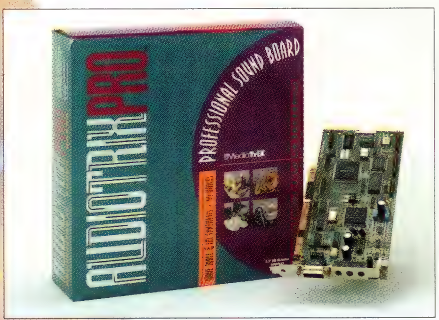

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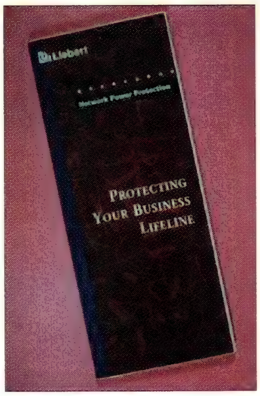

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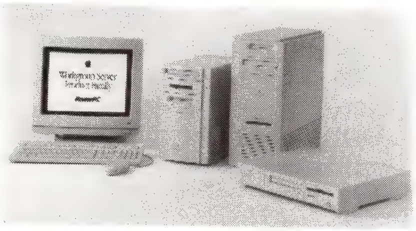
### ▼ SERVERS FEATURE PowerPC CPUs

Two servers, each running with an 80-MHz PowerPC 601 microprocessor, will join the Workgroup Server family—the 8150 at the mid-range and the 9150 at the high end. A third unit, the 6150, employs a 60-MHz 601 processor. The 8150 possesses three NuBus expansion slots, a 1-Gbyte hard-disk drive, a digital-audio tape drive, and support for up to eight SCSI devices. The 9150 offers four NuBus slots, two 1- or 2-Gbyte disk drives, a DAT drive, a double-speed CD-ROM drive, and support for up to 14 SCSI peripherals. Both units feature 16 to 264 Mbytes of DRAM, built-in Ethernet and LocalTalk capabilities, support for AppleTalk networking protocols, and optional Token Ring support. The System 7 operating system is bundled with the servers, as well as AppleShare 4.0.2 file and print server software. The 6150 sells for $4219, the 8150 costs $7459 ($8499 with AppleShare), and the 9150 is priced at $9229 ($10,269 with AppleShare).



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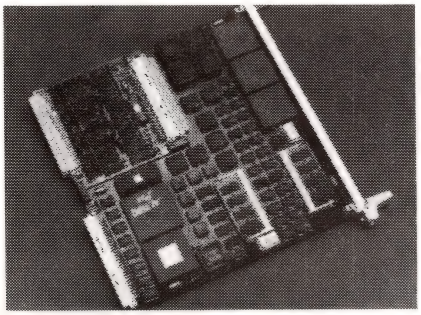
### ▼ MULTIBUS II BOARD HAS EIGHT COMM CHANNELS

Four SAB82525 controllers provide eight communication channels to the HC 486/Lxx Multibus II communication board. Each channel has full-duplex DMA control. The controller's microcode can handle a large set of layer 2 protocol functions independently from the on-board 486 microprocessor. CPU speeds range from 33 to 100 MHz. In addition, time-slot assigning is possible, which makes the board suitable for packet-switching applications. The board's line drivers and receivers are located on a removable interface module that allows all eight channels to be accessed from the P2 connector. Up to 32 Mbytes of DRAM fit on the board, as well as 2 Mbytes of EPROM or 1 Mbyte of flash memory. The HC 486/Lxx supports the iRMX real-time operating system.



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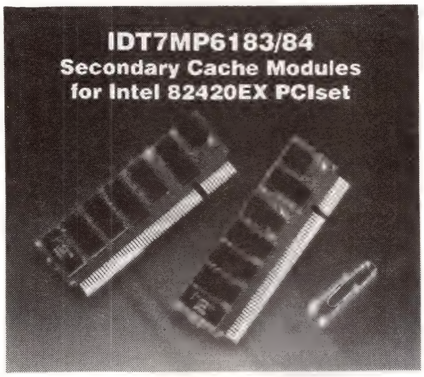
### ▼ CACHE MODULES WORK WITH PCI CHIP SET

Systems that employ a 486 CPU and the Intel 82420EX PCIset core-logic chip set can take advantage of a pair of secondary cache modules. The IDT7MP6183/84 are configured as 128- and 256-kbyte caches that integrate data SRAMs, a cache tag, a buffer, and glue logic onto a 112-pin card-edge module. This module, which offers a 15- or 20-ns access time, takes up just 1 in.$^2$ of board space. Because of the small size, designers can opt to either include extra functionality that wouldn't have fit on board or they can reduce the board's overall size for a cost savings. In lots of 1000, the 128-kbyte 6183 costs $33.10 and the 256-kbyte 6184 is priced at $48.60. Both are available now.



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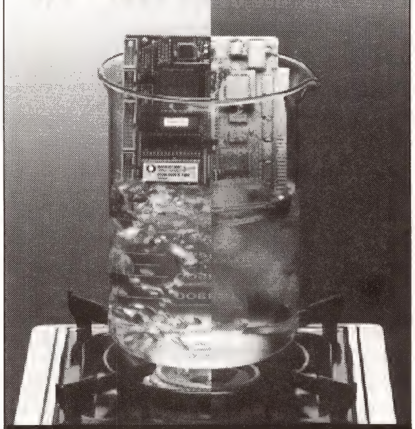

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### ▼ PORTABLE WORKSTATION ADDS 1-GBYTE DISK

The SparcBook 2 workstation-class notebook computer now contains two internal 520-Mbyte hard-disk drives. The SCSI-based drives give users the storage space needed for applications dealing with finance, manufacturing, CAD, CAE, and the military. Other features of the SparcBook 2 include a 40-MHz Sparc processor, up to 64 Mbytes of DRAM, a 64-kbyte cache, and an 8-bit color TFT display. A magnesium-alloy case adds protection and increases the system's heat dissipation while reducing its weight. The system runs a version of Unix that's been altered for portability. It also runs the Solaris operating system. The SparcBook 2 sells for $14,500. Current users can upgrade to the 1-Gbyte model for $3000.

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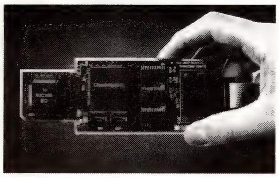

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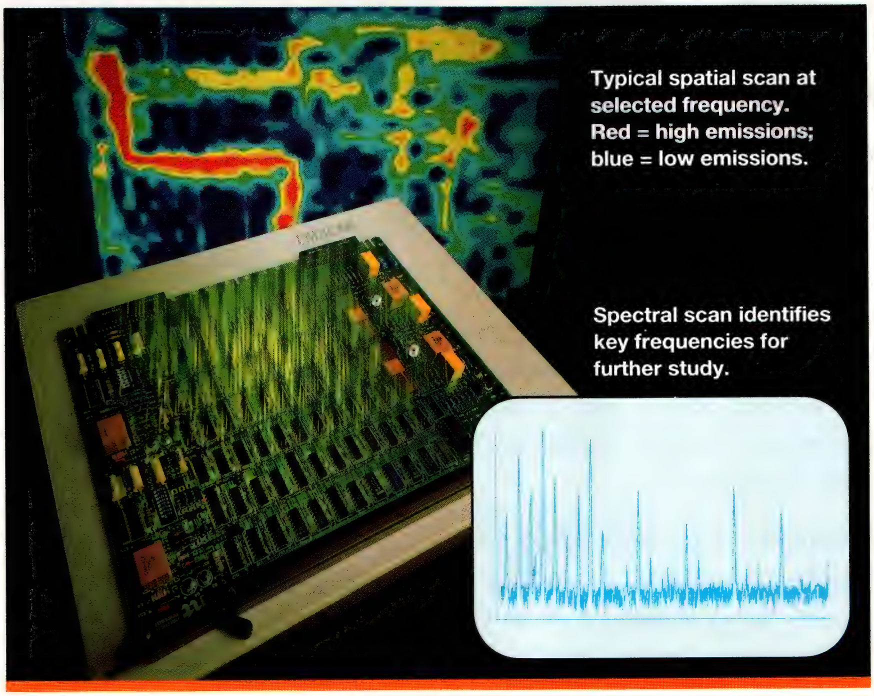
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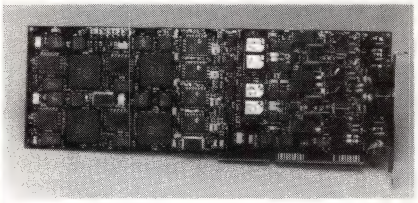
# SYSTEM DESIGN PRODUCTS

## ▼ BROADCAST FAX BOARD OFFERS EASY INTEGRATION

Easy integration of LAN fax capabilities is a key feature of the CP4/LSI board, which facilitates the development of computer-based fax broadcast systems. The board permits direct board-to-phone line connectivity using four built-in loop-start interfaces. With the board's programmability, users can upgrade and scale their systems as their needs change. Other features include a 14.4-kbit/s transmit and receive rate and modified-read data compression. The CP4/LSI sells for $2995.



***GammaLink Inc.***
*1314 Chesapeake Terr.*
*Sunnyvale, CA 94089*
*(408) 744-1400*
**▶CIRCLE 616**

## ▼ CAMERA COMPONENTS HELP INTEGRATE DIGITAL VIDEO

OEM developers looking to integrate video technology into their products will benefit from a series of products, including two camera components and three developer kits. The CDMC-270D8-1 is a one-piece board-level color digital video-camera module; the 270D8-2 is similar, but comes in two pieces. The three kits, called the CAMKIT I, II, and III, each are available with either camera. The CAMKIT I lets engineers create advanced demonstrations and products without the associated host-based analog-to-digital conversion. The CAMKIT II offers an easy way to connect the camera to a PC-based host by capturing images as digital data. The CAMKIT III comes with an output for S-Video that links with VCRs and an output for RGB that interfaces with most color monitors. The camera sells for $495 each, while the CAMKITs I, II, and III sell for $895, $1295, and $1995, respectively.

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*Twice the performance for the same price. I'm telling you Uli, this board is hot.*

*I'm inclined to agree with you, Nick. It's perfect for embedded applications.*

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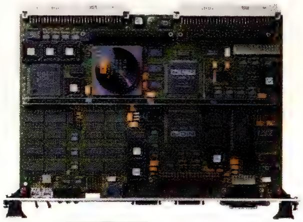
Nick loves our new VME board because it has more than twice the performance of boards that cost just as much. Whereas Uli, being the more levelheaded of the two, appreciates its low price. But then Nick treasures our connection to SUN™ technology. Because deep down he knows that's how we got to market 9 months before anyone else. So engineers–like you, for example–could actually use the new microSPARC™ II technology today. Rather than waiting the usual year. And remember Uli–the levelheaded one? Well he also really loves how compatible our CPU-5CE is with Solaris® and VxWorks.™ And how easy it is to upgrade. But just so you don't think Nick impetuous, you should know that, in the end, he chose FORCE because we had the best technical support in the industry. And you know it's funny, but as different as Uli and Nick are, they both really like being able to call 1-800-FORCE-99 for more information.



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### ▼ PC-COMPATIBLE VME BOARD CONTAINS DX4 PROCESSOR

The Intel DX4 family of microprocessors has made its way into the embedded environment on the EPC-5 board. The 100-MHz VMEbus board, which employs a 33-MHz system bus, can be configured with 4 to 32 Mbytes of memory. For expansion, the board employs a local I/O bus based on the EXM Interface Definition, which is ISA bus-compatible. It holds up to six boards that can be accessed by the VMEbus. This PC-compatible configuration frees the VMEbus for high-speed communications. The EPC-1 sells for $4960 with 4 Mbytes of RAM. Large-quantity discounts apply. Lower speed boards also are available.

***Radisys Corp.***
*15025 SW Koll Pkwy.*
*Beaverton, OR 97006*
*(503) 646-1800*
**▶CIRCLE 618**

### ▼ SYSTEM BOARD HOLDS MULTIPLE PENTIUMS

Multiple Pentium processors can sit on the smp XM board, all running SCO Unix. Up to six Pentiums fit on the board, as well as 256 Mbytes of error-correcting memory and 1 Mbyte of write-back cache for each processor. The board is based on a proprietary bus, called the Extended C-bus. Other operating systems are supported as well, including Windows NT, OS/2, Solaris, and Novell's USL SVR4.2 MP and Netware SFT III. The basic smp XM system, which consists of a 13-slot EISA backplane, sells for under $10,000. Users need only add a chassis, power supply, and peripherals.

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### ▼ 14-IN. COLOR DISPLAY HIGHLIGHTS SYSTEM

The Embedded Control Interface (ECI) series of systems and flat-panel displays includes a 14-in. active-matrix color panel. In a package that's barely 2 in. deep, the systems are built with 486 processors, a PC/104 expansion bus, built-in network capabilities, and fully boot able diskless operation. The systems are designed to mount into OEM cabinets, rack-mount fixtures, and remote enclosures. A slotted mounting frame adjusts to accommodate various front bezel locations. The ECI systems also hold up to 32 Mbytes of DRAM and 2 Mbytes of flash ROM. Monochrome units start at $4100, while the ECI systems with color start at $4995.

***Dolch Computer Systems***
*372 Turquoise St.*
*Milpitas, CA 95035*
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### ▼ 6U VME BOARD HOLDS 85-MHz SPARC CPU

A single-slot 6U VMEbus board can supply the performance of a SparcStation 10 workstation. The board, called the Sparc CPU-5CE, is based on the microSparc II processor. The 85-MHz processor integrates the integer and floating point units with the MMU, 16 kbytes of instruction cache, 8 kbytes of data cache, memory control, and an SBus interface. The board supplies 85 MIPS and 34 MFLOPS. It holds up to 64 Mbytes of DRAM and supports two SBus modules. Support is included for the Solaris 1.1 and 2.3 operating systems as well as the VxWorks real-time operating system. A 16-Mbyte board sells for $4995 in single quantities.

***Force Computers Inc.***
*2001 Logic Dr.*
*San Jose, CA 95124*
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1
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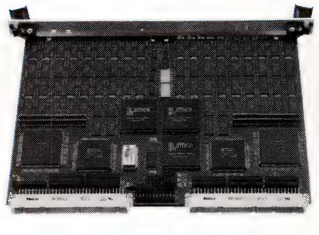

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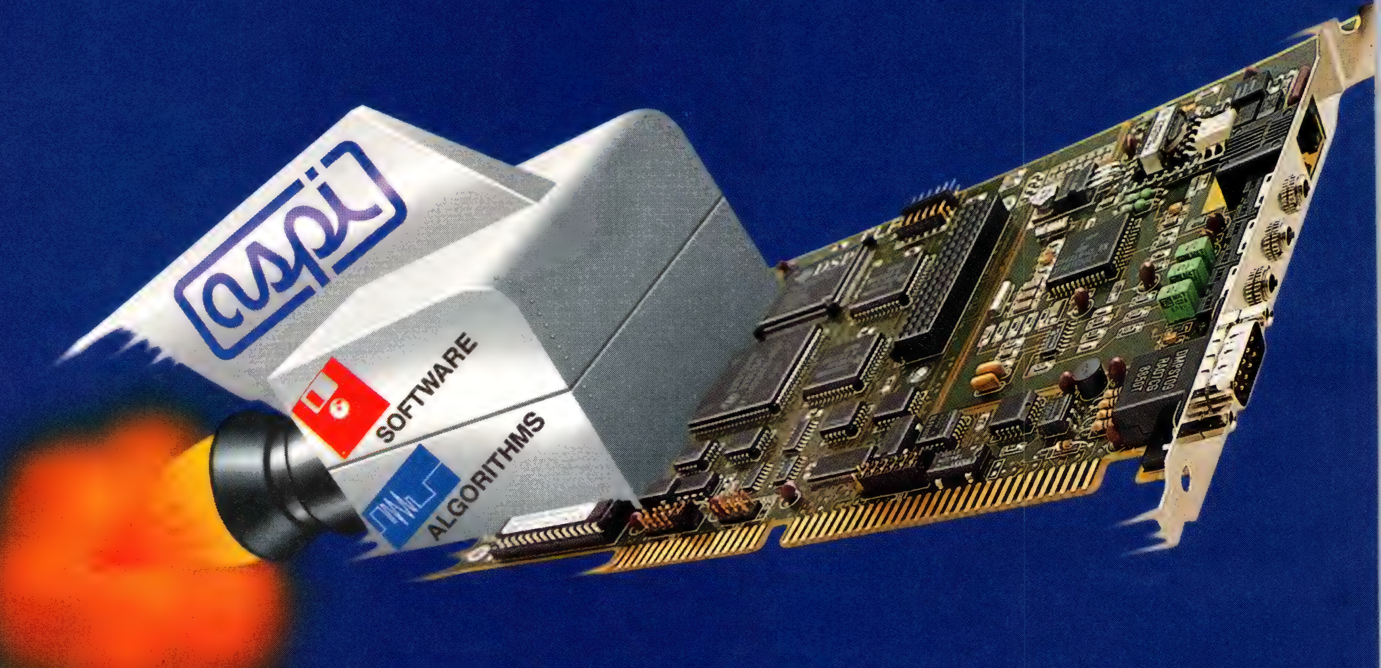
# Elf Launches DSP Applications!



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If you are considering DSP for your applications, the Elf Application Toolkit is now available. The Evaluation Toolkit includes the Elf DSP Platform and demos of many DSP algorithms, including those found in the Developer's Toolkit. Contact Atlanta Signal Processors, Inc. today for complete details.

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# VME BOARDS COMBINE PCI BUS AND POWERPC CPUS

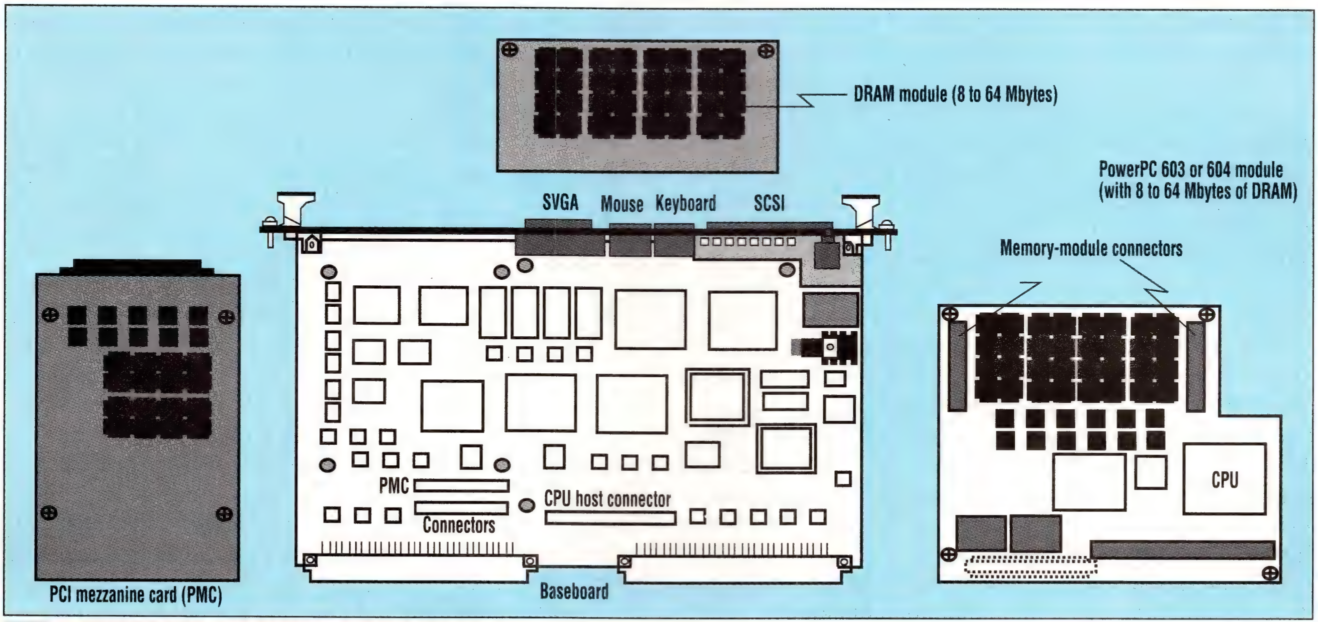
## THE MODULARITY OF SINGLE-BOARD COMPUTERS LETS USERS SWAP CPUS, MEMORY, AND I/O TO SUIT THE APPLICATION.

**RICHARD NASS**

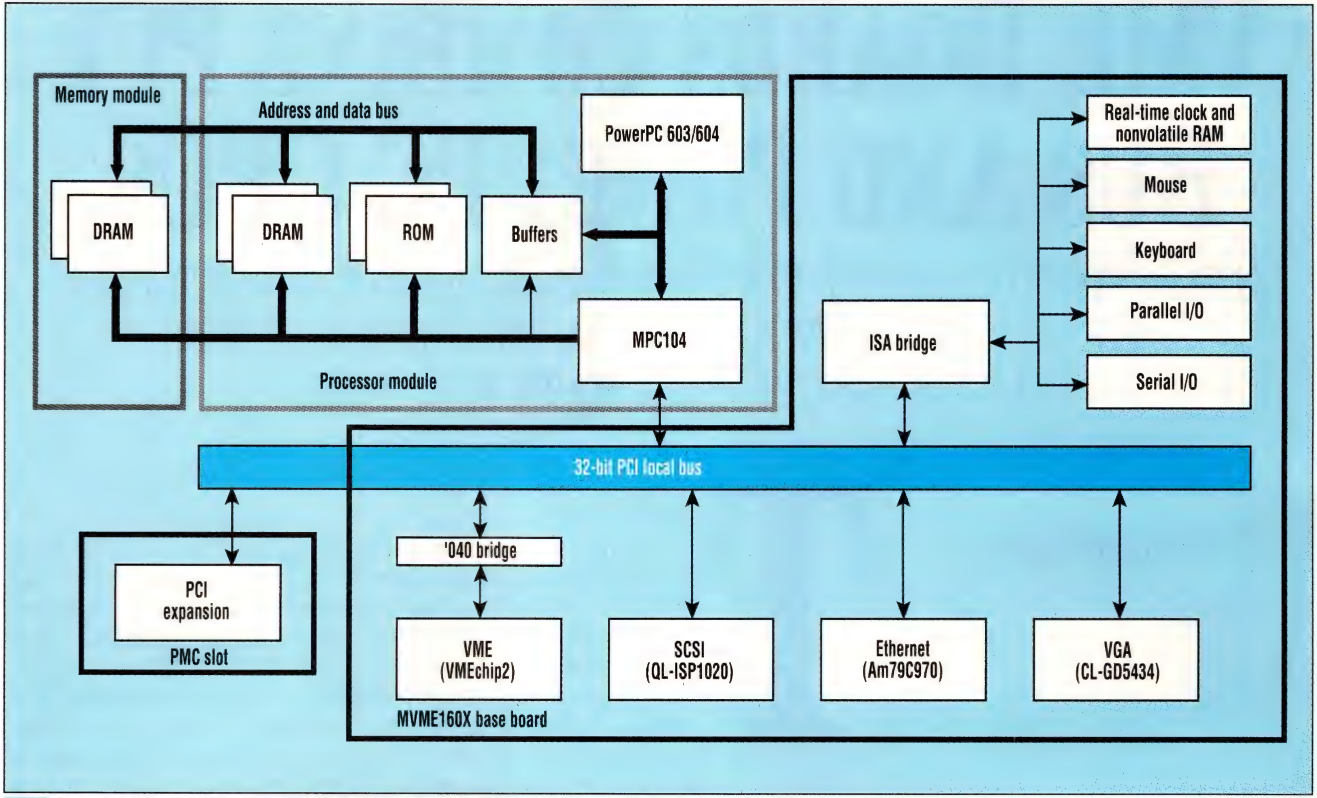
The Peripheral Component Interconnect (PCI) bus has made great strides in easing system-level data-transfer bottlenecks. Moreover, the PCI local bus has been instrumental in the movement of data between memory and peripheral controllers. Now that capability is being added to powerful board-level computers, thanks to a pair of VMEbus boards introduced by Motorola's Computer Group. The boards are based on the PowerPC microprocessor family (this comes on the heels of Motorola's unveiling of a VMEbus board based on the company's 68060 microprocessor). The two new boards are the MVME1603 and MVME1604, built with the PowerPC 603 and 604 processors, respectively. Their mezzanine architecture is based on the standard PCI local bus.

The primary targets for the modular family are embedded monitoring and control applications. The MVME1603 is aimed at mid-range applications, delivering performance ratings of 55 SPECint92 and 70 SPECfp92. The MVME1604, which is geared toward higher-end applications, pushes those numbers to 140 SPECint92 and 145 SPECfp92.

Customization is possible due to the PCI connection's modularity. In addition,



**1. THE TWO MVME160X BOARDS** employ a similar baseboard. Users can add a number of devices to the baseboard, such as a memory module (with 8 to 64 Mbytes of DRAM) and a PCI mezzanine card. Then, either a PowerPC 603 or 604 CPU card, which also holds 8 to 64 Mbytes of DRAM, is plugged in. Even with the modules, the board still fits a one-slot VME form factor.



**2. THE PCI BUS CONNECTS TO THE PROCESSOR** through a bridge chip (the MPC104). The interface options, including the VME, SCSI, Ethernet, and VGA, all hang off the PCI bus.

the CPUs and memory plug into a similar base board, letting users choose the desired options and performance level *(Fig. 1)*. The PCI bus actually connects to the processor through a bridge chip, the MPC104.

Both microprocessors are built with an advanced 3.3-V CMOS process. The PowerPC 603 32-bit superscalar RISC processor can execute up to three instructions per clock cycle. And although those instructions can execute out of sequence, the chip makes the completion appear sequential. The part, which runs at 66 MHz, consists of five integrated components in addition to the dual 8-kbyte caches: an integer unit, a floating-point unit, a branch-processing unit, a load and store unit, and a system register unit.

The MVME603 board is built with a selectable 32- or 64-bit data bus and a 32-bit address bus. Its interface protocol allows multiple masters to compete for system resources through a central arbiter. A three-state coherency protocol supports the exclusive, modified, and invalid cache states.

The PowerPC 604 microprocessor is similar to the PowerPC 603, yet its clock rate is 100 MHz and it can process four instructions simultaneously. As many as six instructions can finish execution in parallel. In addition, it has three integer units—two single cycles and one multiple cycle.

Both CPUs contain a low-power mode where all internal processing and bus operation is suspended and the internal clocks are powered down. All that remains active is a decrementer and time-base and interrupt logic. Any asynchronous interrupt can wake the CPU.

The 604 contains two 16-kbyte cache memories. It also incorporates multiprocessor support, such as support for bus snooping, data-cache coherency, and a high-speed secondary-cache memory.

## PCI To PMC

The mezzanine employed on the boards is called a PCI Mezzanine Card (PMC) connection. It's actually a subset of the PCI specification, offering a lower profile than the standard PCI modules.

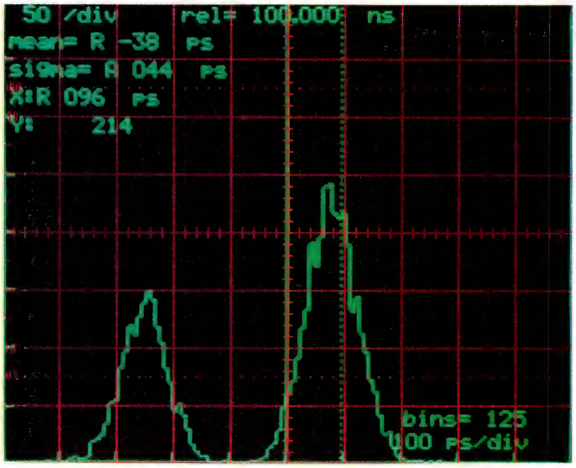
The PCI bus is used as a local connection between the processor-memory array and the system peripheral controllers *(Fig. 2)*. The PMC is defined under the IEEE's P1386.1 specification.

The scope of the IEEE P1386.1 specification is to define a family of cards for VMEbus, Futurebus+, and other high-end systems. But the 4.2-by-12.3-in. board defined by the popular PCI specification (which plugs into the baseboard in a perpendicular fashion) wouldn't fit the form factor of a single-slot VMEbus board. Hence, the PMC specification evolved, using electrical and logical layers that are similar to PCI (though there are physical differences).

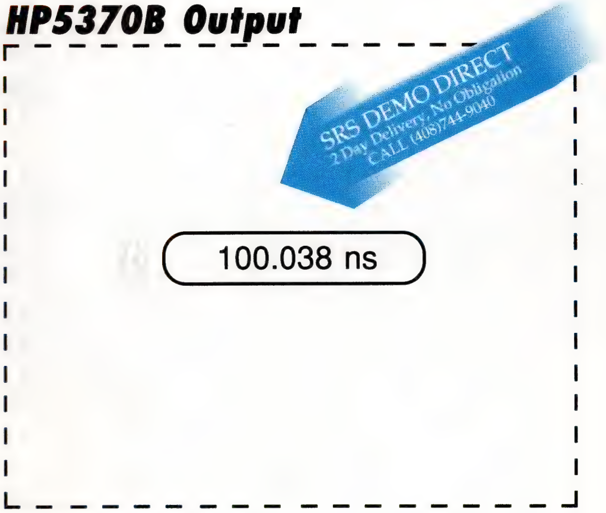
A VME board that contains a PMC module still fits the VME form factor in one slot. The PMC's high bandwidth can transfer 132 Mbytes/s in a 32-bit mode and 264 Mbytes/s using 64 bits. On the MVME160X family, the module can connect either through the baseboard's front panel or the P2 connector. According to Motorola, the available modules will include support for graphics, the Fiber Distributed Data Interface (FDDI), asynchronous transfer-mode (ATM) communications, and other high-performance I/O peripherals.

# A picture is worth a thousand points in a time interval measurement.

## SR620 Output



## HP5370B Output



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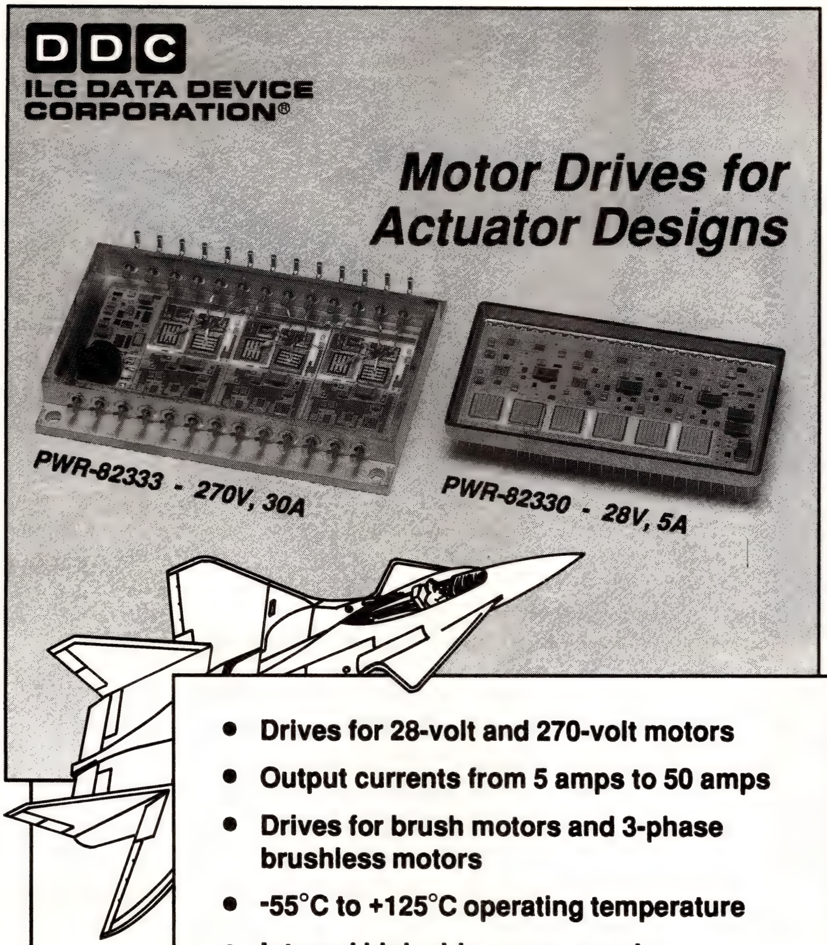

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## POWER PC-PCI VME SBC

The VMEbus baseboards can handle from 8 to 64 Mbytes of DRAM. Expansion modules are available so that users can upgrade to 128 Mbytes without taking another slot.

VME interface functionality is supplied by the VMEchip2 ASIC. In addition to controlling the board's VMEbus functions, the chip includes a local-bus-to-VMEbus DMA controller, and a global control and status register for interprocessor communications.

### ADDITIONAL I/OS

Apart from the 33-MHz PMC connection, peripheral I/O connections are located on the front panel and the P2 connector. The 16-bit fast and wide SCSI-2, Super VGA graphics, mouse, and keyboard connections are on the front panel. Serial, parallel, and Ethernet connections reside on the P2 connector and require a transition module to interface with standard connectors. Support for a VME64 interface also improves performance.

Both the MVME1603 and MVME1604 boards are available with many development tools. Development software for the MVME160X family incorporates on-board debugger and monitor firmware, as well as driver packages for the VME environment. Object and source code is available for application development.

Several real-time operating systems and kernels, in addition to Motorola's VMEexec operating system, are included to support the boards. Among the systems are the LynxOS from Lynx Real-Time Systems, the OS-9 from Microware Systems, pSOS+ from Integrated Systems, VRTX from Microtec Research, and VxWorks from Wind River Systems. ☐

### PRICE AND AVAILABILITY

*The MVME1603, based on a 66-MHz PowerPC 603 microprocessor, costs $3575 and will be available in September. The MVME1604, which holds a PowerPC 604 CPU, will be available in November for $4575. Each board has 8 Mbytes of DRAM.*

*Motorola Computer Group, 2900 South Diablo Way, Tempe, AZ 85282; (800) 759-1107.* **CIRCLE 512**

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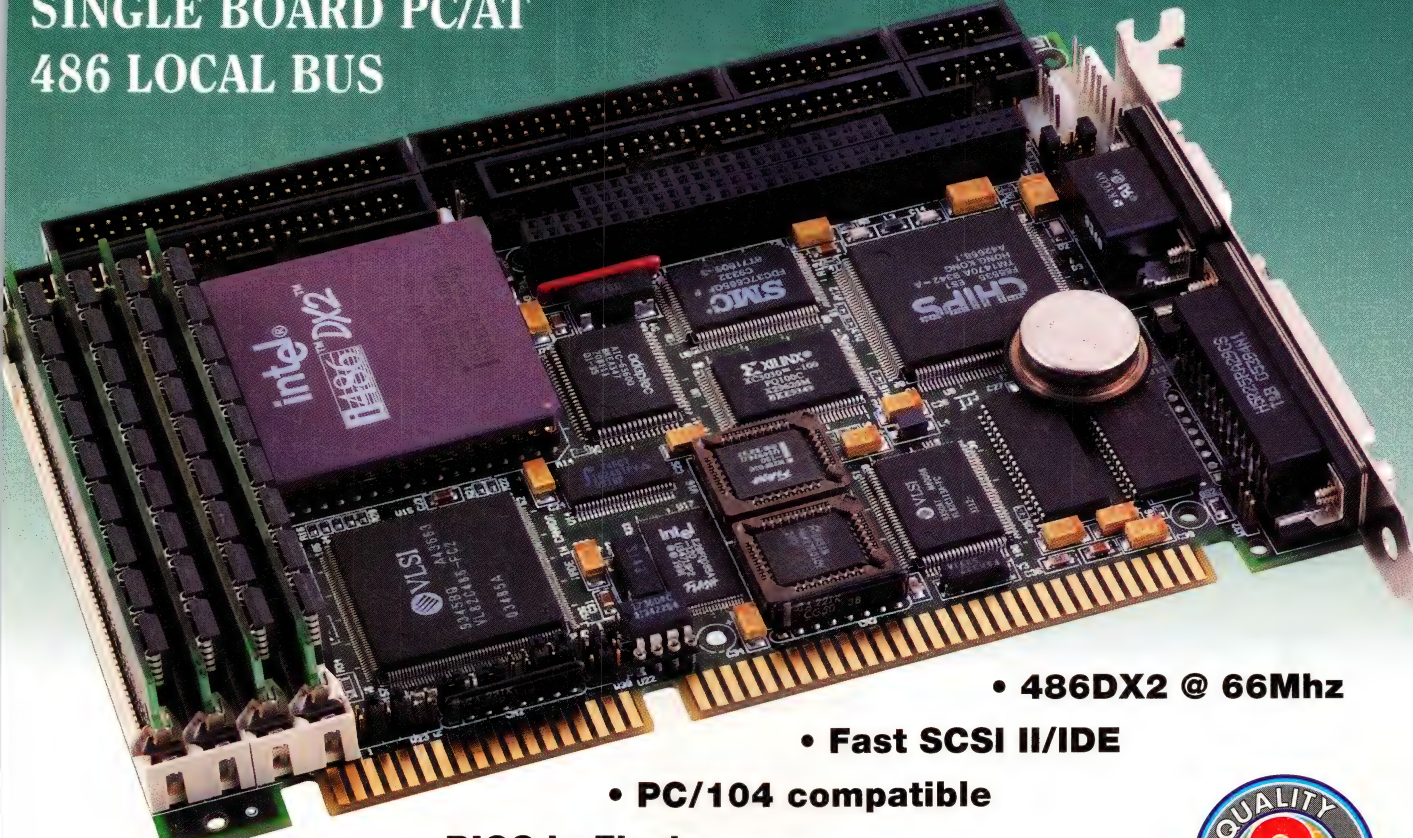

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TO-5 RELAY TECHNOLOGY

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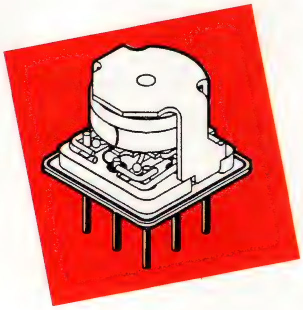

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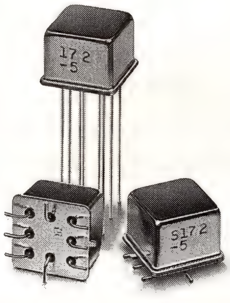

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READER SERVICE 127

# EMBEDDED i960 CPU OFFERS 45 VAX MIPS

## 3.3-V OPERATION, CLOCK-DOUBLING TECHNIQUES, AND LARGE INTERNAL CACHES HIGHLIGHT 32-BIT RISC CPU CHIP.

RICHARD NASS

Embedded RISC microprocessors have really hit their stride over the last few years, finding their way into applications ranging from office-automation devices to consumer electronics to automotives. One of the leaders of the embedded CPU trend is the i960 family hailing from Intel Corp., Santa Clara, Calif.

A new member—the 80960JF—now has joined the family *(Fig. 1)*. With a rating of 45 VAX MIPS, the CPU offers a performance level that's four times better than the previous generation, the i960KA. At 5 V, the chip runs at 40 MHz (a forthcoming version will reach 50 MHz). At 3.3 V, it can still run at 33 MHz.

The 32-bit i960JF is object-code-compatible with other members of the family. It also incorporates several new features to enhance performance and make it easier to use. The CPU chip can sustain execution at one instruction per clock cycle. Register and resource scoreboarding permit overlapped instruction execution.

Optimized for C-language operation, the 80960JF (also called the i960JF) adds a number of instructions to the family's core, giving the program a simpler and more efficient flow. The new instructions include conditional move, add, subtract, halt, cache control, and interrupt control.

The processor core employs Intel's popular clock-doubling technique. This means the chip runs twice as fast internally as it does externally. It contains an independent multiply-and-divide unit and an efficient pipeline that minimizes latencies. Memory subsystems for cost-sensitive embedded applications often impose substantial wait-state penalties.

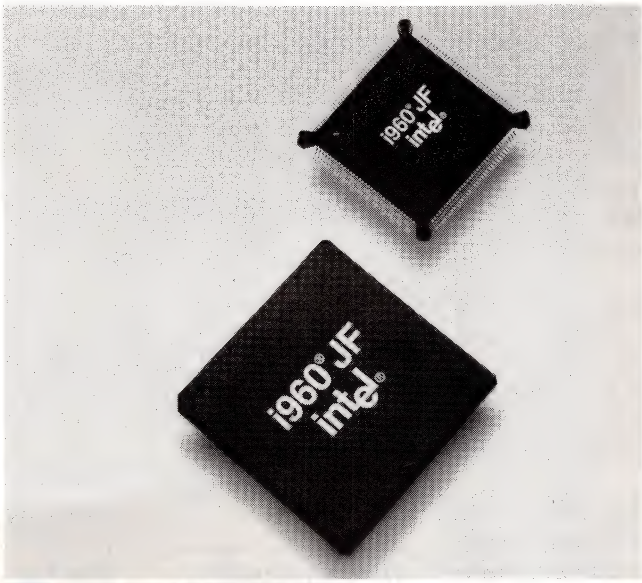
Considerable storage resources are integrated on-chip to decouple CPU execution from the external bus. Included are 4 kbytes of two-way, set-associative instruction cache, 2 kbytes of direct-mapped data cache, and 1 kbyte of data RAM for program storage. An eight-set stack-frame cache lets the processor rapidly allocate and deallocate local registers during context switches.

A 32-bit multiplexed burst bus supplies a high-speed interface between the system memory and the peripherals. A full complement of control signals simplifies the connection between the CPU and the external components.

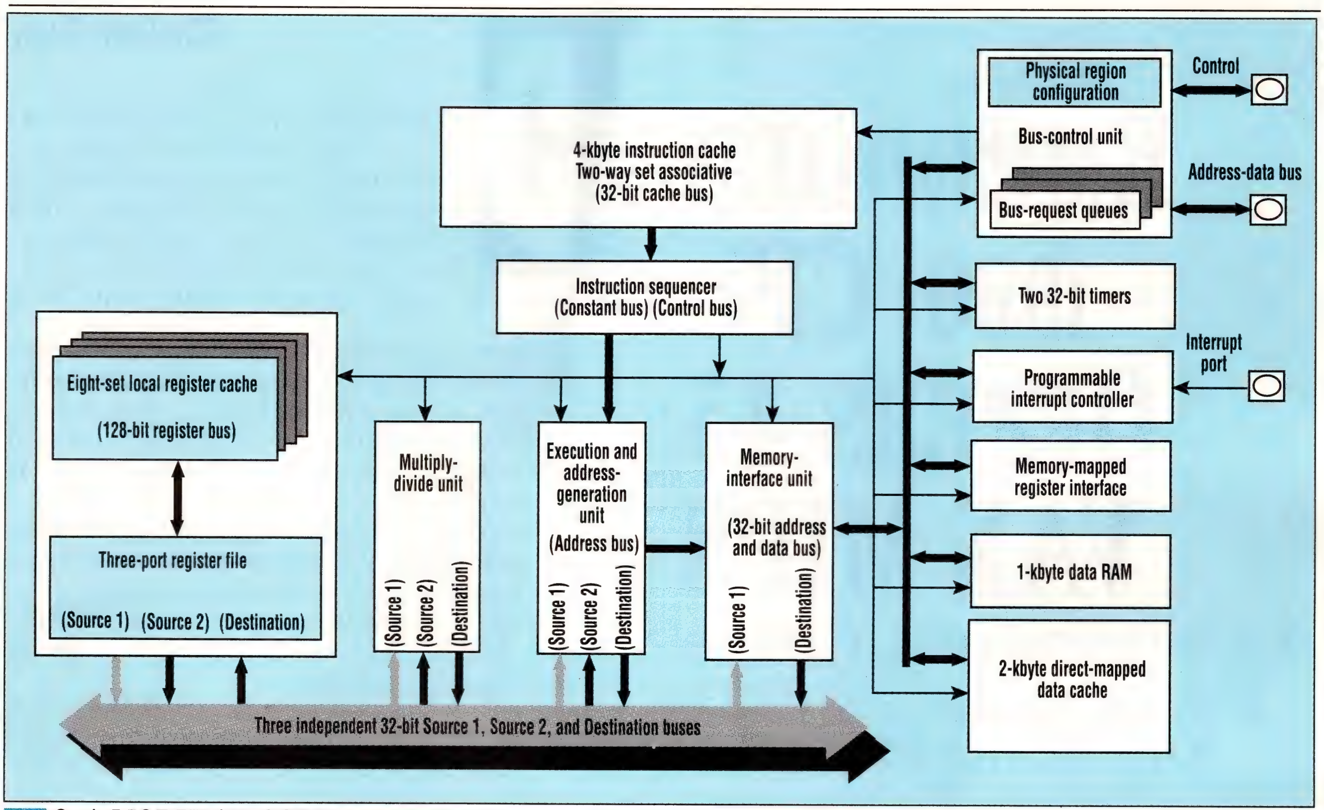
Users can program the physical as well as the logical memory attributes through memory-mapped control registers, which lets the processor operate with all combinations of bus-width and data-object alignment. In addition, the processor supports a homogeneous byte-ordering model.

The bus-control unit fetches instructions and transfers data at up to four 32-bit words per every six clock cycles. The external address and data bus is multiplexed. The processor's memory space can be configured for logical characteristics to match an application's requirements. The physical bus width can be register-programmed for up to eight regions. Byte ordering and data caching are programmed through a group of templates and a default register.

Other features of the bus-control unit include a multiplexed external bus to minimize pin count; 8-, 16-, and



**1. COMPARED TO THE** previous generation, Intel's latest 32-bit embedded RISC microprocessor, the 80960JF, delivers four times the processing power. The clock-doubled 80960JF pumps out 45 VAX MIPS.


Physical region configuration
Bus-control unit
Bus-request queues
Control
Address-data bus
4-kbyte instruction cache
Two-way set associative
(32-bit cache bus)
Instruction sequencer
(Constant bus) (Control bus)
Two 32-bit timers
Interrupt port
Programmable interrupt controller
Memory-mapped register interface
1-kbyte data RAM
2-kbyte direct-mapped data cache
Eight-set local register cache
(128-bit register bus)
Three-port register file
(Source 1) (Source 2) (Destination)
Multiply-divide unit
(Source 1)
(Source 2)
(Destination)
Execution and address-generation unit
(Address bus)
(Source 1)
(Source 2)
(Destination)
Memory-interface unit
(32-bit address and data bus)
(Source 1)
(Destination)
Three independent 32-bit Source 1, Source 2, and Destination buses

**2. A MODULAR CORE** highlights the design of the i960JF 32-bit embedded RISC processor. This includes a local register cache, instruction and data caches, and data RAM for reduced memory accesses and bus traffic. The CPU also contains an enhanced bus-control unit to handle multiple data types.

32-bit bus widths to simplify I/O interfaces; and external ready control for address-to-data, data-to-data, and data-to-next-address wait states. The unit also supports big- and little-endian byte ordering to facilitate porting existing program code. It can transparently perform unaligned bus accesses, and features a three-deep load-and-store queue to decouple the processor's bus from its core.

## INTEGRATED PERIPHERALS

Two important peripherals are integrated onto the chip—a timer unit and an interrupt controller. These resources can be programmed through memory-mapped control registers. The timer unit contains two independent 32-bit timers that can be used as real-time clocks or general-purpose system timing. The timers can operate in single-shot or auto-reload modes and generate interrupts to the core. Also, the timers can operate at several different clock rates.

The programmable interrupt controller offers full programmability of up to 248 interrupt sources into 32 priority levels through an 8-bit external interrupt port. Alternatively, the interrupt inputs can be configured for individual edge-triggered or level-triggered inputs.

The controller also accepts interrupts from the two on-chip timer channels and a single non-maskable interrupt pin. Interrupts are serviced according to their priority levels, relative to the current process priority. The interrupt mechanism takes advantage of a cached priority table, dedicated local registers, and cached interrupt routines to minimize interrupt latency.

A wide variety of tool support is available for the chips. This includes compilers, real-time kernels, boards, emulators, simulators, and logic analyzers. In addition, software support is included for Unix, DOS, and Windows hosts.

Also incorporated into the chip are advanced testability features, including chip and system testing, a built-in self test, and on-chip break-point capabilities for software developers. The self-test feature checks the basic functionality of internal data paths, registers, and memory arrays. The hardware breakpoints are tested using two instruction and two data-address registers. The registers are compatible with standard software debuggers.

Two package options are available for the 80960JF RISC processor: a 132-lead pin-grid array or a 132-lead plastic quad flat pack. The device is fabricated on a 0.8-µm CMOS process, which helps reduce power consumption. ☐

## PRICE AND AVAILABILITY

*The 5-V 80960JF will sample in September and go into production in December. The 3.3-V version is scheduled to sample in December, with large-volume quantities available next March. Prices for the i960JF series of embedded RISC microprocessors start at $24.90 in quantities of 10,000. In addition, processors with smaller and larger caches and higher clock frequencies will be available early next year.*

*Intel Corp., 5000 W. Chandler Blvd., Chandler, AZ 85226; (800) 628-2283.*

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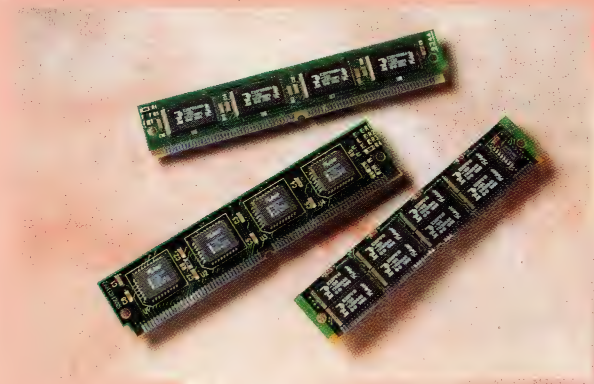

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READER SERVICE 124

# DON'T GET *ZAPPED*!

## Make the Intelligent Choice by Knowing

**Can the IC latch up if hit with ESD?**
This is critical. An ESD event may cause the ESD structure to latch, in which case the IC would stop functioning and use up to 1A of current until system power is recycled. In severe cases, the IC could burn up, rendering the serial port useless.

**What is the ESD voltage rating and test method?**
Different test methods yield different voltage ratings. Maxim specifies its high ESD RS-232 ICs using the Human Body Model and IEC 801-2 (Contact and Air Gap Discharge).

**What were the test results over the complete ESD protection range?**
ESD protection structures are dynamic in nature—different mechanisms operate at different voltages. Therefore, a device that survives a ±10kV Human Body Model (HBM) ESD pulse may not survive a ±5kV HBM ESD pulse. Maxim tests ESD over the entire voltage range in 200V increments.

For applications assistance, call 1-800-998-8800

## Differences Between IEC 801-2 and the Human Body Model

The main difference between the two ESD standards is the peak current. A device zapped using IEC 801-2 must absorb over five times more peak current for the same voltage, compared to the Human Body Model:

| VOLTAGE (kV) | PEAK CURRENT | |
|---|---|---|
| | IEC 801-2 (A) | HUMAN BODY MODEL (A) |
| 2 | 7.5 | 1.33 |
| 4 | 15.0 | 2.67 |
| 6 | 22.5 | 4.00 |
| 8 | 30.0 | 5.33 |
| 10 | 37.5 | 6.67 |

# SELECT THE RIGHT HIGH ESD RS-232 IC!

## the Facts About ESD Protection

**Does the ESD protection affect normal operation?**
In normal operation, an improperly designed ESD structure could trigger, causing latchup. For RS-232 ICs, a slew rate of less than 3V/µs indicates that the device may be susceptible to latchup.

**Are there any special precautions that must be taken to use the IC?**
Some bipolar ICs may need expensive, low-ESR capacitors, or a low-impedance AC ground path to function. It's best to know what you're getting into beforehand.

MAXIM

## Select the Rugged, ±15kV ESD, +5V RS-232 IC for Your Design

| MAXIM PART | Tx/Rx | ESD* | | | LATCHUP FREE | CAPACITORS (µF) | DATA RATE (kbps) | PRICE† |
|---|---|---|---|---|---|---|---|---|
| | | HUMAN BODY MODEL | IEC801-2 | | | | | |
| | | | CONTACT DISCHARGE | AIR GAP DISCHARGE | | | | |
| MAX202E | 2/2 | ±15kV | ±8kV | ±15kV | YES | 0.1 | 120 | $1.85 |
| MAX232E | 2/2 | ±15kV | ±8kV | ±15kV | YES | 1.0 | 120 | $1.85 |
| MAX211E | 4/5 | ±15kV | ±8kV | ±15kV | YES | 0.1 | 120 | $3.62 |
| MAX213E | 4/5 | ±15kV | ±8kV | ±15kV | YES | 0.1 | 120 | $3.62 |
| MAX241E | 4/5 | ±15kV | ±8kV | ±15kV | YES | 1.0 | 120 | $3.62 |

**ESD testing done on all RS-232 I/O pins using Human Body Model waveform and IEC 801-2 waveform.*
*†Price is 1000 piece recommended resale.*

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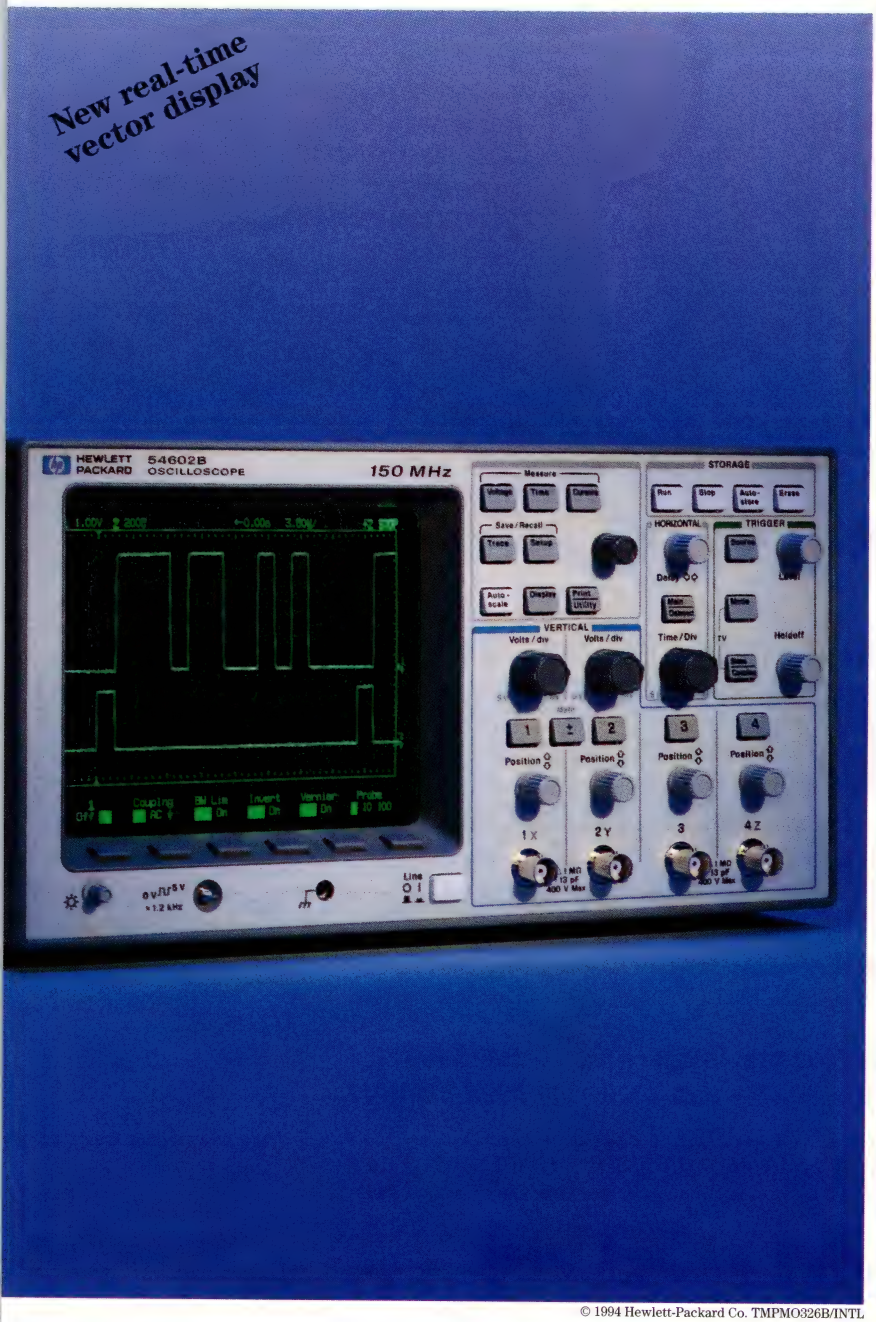

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READER SERVICE 96

# FAST ADC ENABLES DIGITAL BASEBAND RF TECHNOLOGY

ONCE THE PROVINCE OF THE MILITARY AND INTELLIGENCE COMMUNITIES, DIGITAL RF FINALLY "COMES IN FROM THE COLD."

**FRANK GOODENOUGH AND LEE GOLDBERG**

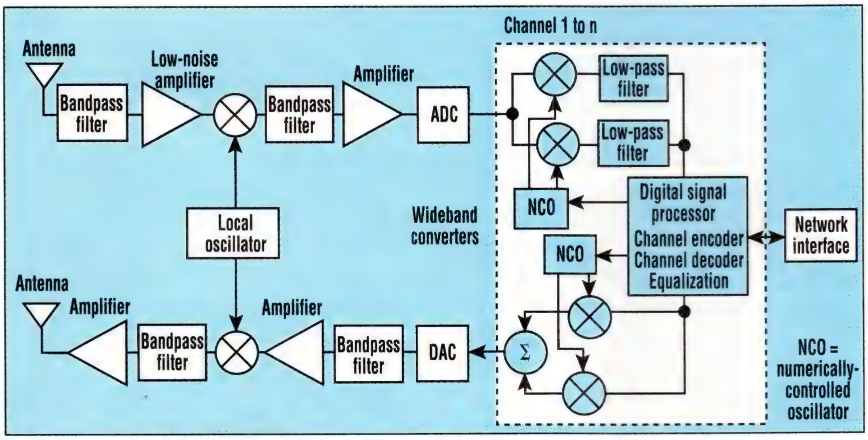
Is the superheterodyne receiver doomed like the vacuum tube that originally made it possible? The newest generation of analog-to-digital-converter (ADC) technology seems to point in that direction, because it's capable of rapidly obsoleting analog IF signal processing at frequencies below 15 MHz. If this high-speed conversion technology proves viable, virtually all RF communication links may soon carry only *digital* baseband signals—strings of ones and zeros waiting for further processing by the soon-to-be-ubiquitous digital signal processor.

Instead of using a heterodyne process, baseband signals now can be extracted from the carrier frequency by directly digitizing the output of an RF receiver's IF stage for further processing in digital or analog form. While the process of IF digitization has been feasible for some time, the high-precision ADCs required to capture a 15-MHz IF signal cost thousands of dollars, making commercial applications of digital baseband technology impractical.

One company, Analog Devices, has now changed this situation. It has developed an advanced 12-bit, 31-MHz ADC. This product is part of the company's strategy to become a leading supplier of the next generation of communication system components. Such components will make use of highly-integrated digital-signal-processing (DSP) technology *(Fig. 1)*.

To develop one of the important building blocks of this system, Analog Devices worked closely with several communications equipment manufacturers, including the Steinbrecher Corp., Burlington, Mass. From this collaboration came a pair of monolithic 12-bit ADCs with sufficient speed and precision for digital IF applications—the AD9026 (for TTL signals) and the AD9027 (for ECL signals).

Both converters feature a sampling rate of 31 MHz and impressive dynamic performance. While digitizing a 13.4-MHz signal at its maximum sample rate of 31 MHz, each converter boasts a signal-to-(noise + distortion) ratio-SINARD-of 62 dB. Each ADC delivers a total harmonic distortion-THD-of 70 dBc (an 11.3-bit effective resolution) over the full industrial-temperature range. At a temperature of 25°C, their spurious-free dynamic range-SFDR-runs 72.1 dB, yielding an equivalent digital resolution of about 11.7 bits. Two-tone intermodulation distortion is typically about 73 dBc at input frequencies of 9.6 and 11.3 MHz.



**1. THIS ALL-DIGITAL BASE STATION architecture is Analog Devices' vision for cellular telephone-system infrastructures of the future. Once signals are mixed down to the IF, the entire spectrum of interest is sampled by a high-speed ADC (Analog Devices AD9026/7), resulting in every channel being digitized simultaneously. All tuning and demodulation is done in the digital domain, using dedicated DSP hardware running at the ADC's sampling rate. Narrow-band decimation filters extract each channel from the data stream for further processing by a dedicated DSP IC.**

## INNOVATIVE ARCHITECTURE

To attain these tough requirements, the ADCs employ an innovative three-pass subranging architecture. Its two track-and-hold (T/H) amplifiers, three flash ADCs, two digital-to-analog converters (DACs), and two residue amplifiers produce a 14-bit digital word that's reduced to a 12-bit word by digital error correction *(Fig. 2)*. The input T/H amplifier is the most critical block, because it must sample a ±1.024-V signal—to 12-bit accuracy—at 31 Msamples/s. The T/H-amplifier's errors are *not* eliminated by the digital-error-correction circuits. The DAC located at the output of the first 5-bit ADC also must be 12-bit accurate.

The analog input signals are attenuated through a resistive divider and applied to the T/H amplifier's sampling bridge. It holds the analog voltage present when the Encode input is strobed.

The voltage held by the T/H amplifier also is applied to a 5-bit flash ADC and a second T/H amplifier. The first flash ADC produces the 5 most-significant bits (MSBs), which are then reconstituted by a 5-bit DAC and subtracted from the first T/H-amplifier output to form a residue signal.

The second T/H amplifier samples this residue signal, which is then passed on to a gain-of-16 amplifier and a second 5-bit flash ADC. The latter ADC's 5-bit output is reconstituted by a second 5-bit DAC, which is subtracted from the output of the second T/H amplifier to form a second residue signal. This second-residue signal is given a gain of eight and applied to a 4-bit flash ADC. As noted earlier, the digital-error-correction logic aligns the 14-bit data from the three ADCs to form the 12-bit parallel output digital word.

Much of the converter's high-end accuracy is due to the excellent characteristics of the T/H amplifiers used in its front end. The analog bandwidth of the input T/H amplifier typically runs over a wide band of 200 MHz, making the AD9026/9027 applicable to undersampling frequencies well above the Nyquist point.

According to Analog Devices, without the help of their customers in designing the input T/H amplifier, the ADCs could not have been realized. Actually, Steinbrecher had implemented the sampling function using discrete components, but later realized that a monolithic solution was needed to make the system economically viable.

The ADCs have excellent SFDR characteristics. Such a feature over the full Nyquist bandwidth ensures successful multichannel receiver applications at up to a frequency of 15 MHz.

Unlike many wideband ADCs, the dc specifications of these units need no apology. No-missing-code operation is guaranteed to 12 bits. Differential and integral nonlinearity errors run a maximum of 1 and 3 least-significant bits (LSBs), respectively. Furthermore, all three specifications hold over the entire operating-temperature range.

## MANY APPLICATIONS

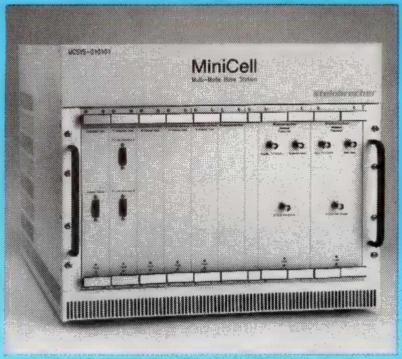
A moderate-cost converter with such exceptional specifications opens up a wide variety of applications that were previously cost-prohibitive. By digitizing the baseband directly, one receiver can take in a portion of the

## ADVANCED DSP TECHNOLOGY DRIVES LOW-COST CELLULAR BASE STATION

By combining digital baseband technology and high-performance ICs, engineers at the Steinbrecher Corp. were able to design first-generation low-cost cellular radio products that will reduce the cost of a typical base station by up to 80%. Until recently, the company was small, producing highly sophisticated government and military receivers and RF mixers for over-the-horizon radar and Milstar satellite transceivers. With declining defense and intelligence spending, Doug Shute, Steinbrecher's president and c.e.o., looked to the growing cellular telephone industry as an area of great opportunity.

During the late 1980s, Steinbrecher experimented with using DSP technology to monitor cellular-telephone traffic for a government agency. One of the things that gave the firm's products such excellent performance was a unique broadband mixer technology, dubbed "Paramixer" by the company's founder Don Steinbrecher. Instead of translating a single channel from its carrier frequency to the IF, the Paramixer takes a very wide slice of a communication spectrum (typically 10 to 100 MHz compared to 10 to 100 kHz for conventional radios) down to baseband while introducing virtually no distortion into the signal under scrutiny. The entire band which contains several channels is digitized and sent over a data bus to a bank of DSP ICs. Each processor then extracts and decodes one channel from the passing bit-stream.

Using broadband processing, only one RF transceiver and digitizing stage is needed to feed the digital filters and signal processors that separate the individual channels and demodulate them. Outgoing traffic is digitally combined into a baseband signal and brought up to the carrier frequency as a single wide channel. This substantially reduces the volume and cost of equipment required for a cellular base station. Once the broadband mixer



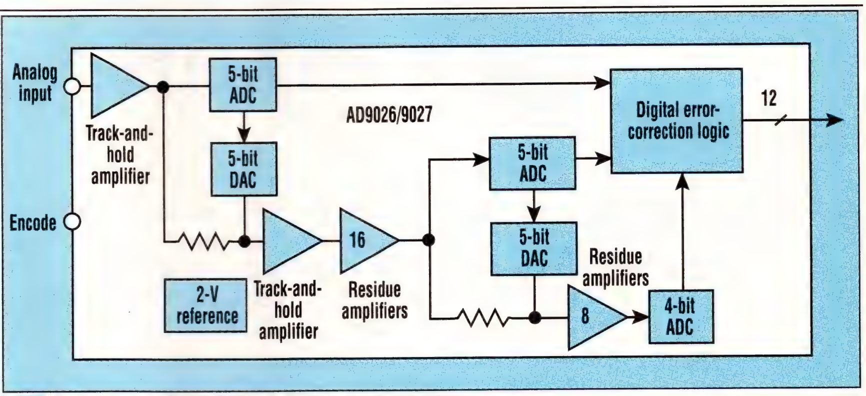
was coupled to recent developments in low-cost DSP, the Minicell concept was born.

At around $100,000, the MiniCell costs about 10% of a conventional base station. Its very small size eliminates real-estate and housing costs associated with conventional base stations *(see the figure)*. Also, the low cost will allow cellular service providers to employ it in new ways to boost network performance. As an example, a MiniCell transceiver can be used as a cost-effective capacity enhancer to cover geographic dead zones or to provide spectrum, digitize it, and pass it to any number of channel processors via a digital data bus.

Besides the drastic reduction in component count, this lends itself to application of advanced DSP techniques. Though used in advanced military equipment for some time, one of the technology's first civilian applications is in a cellular telephone base station developed by the Steinbrecher Corp. *(see "Advanced DSP technology drives low-cost cellular base station," p. XX).*

The ADC is the key to Steinbrecher Corp.'s MiniCell digital transceiver system. Used as a cellular-telephone base station, the MiniCell concept makes it possible to reduce conventional cellular-telephone base-station costs by as much as 90%. This further leads to the possibility of developing low-cost, wireless, private-area branch-exchange (PABX) telephone systems.

Scheduled for production in early 1995, the MiniCell digital transceiver system can be used in a variety of ways to build a low-cost and flexible cellular communications infrastructure. Used as a base station, each transceiver typically handles 24 of the 416 cellular channels. To expand channel capacity, additional DSP channels may be added to the system. The system's programmable signal processors permit the station to support any mix of transmission technologies, giving carriers the ability to handle digital as well as analog traffic with the same hardware. And thanks to its small size and digital interface, remote operation from rooftops or utility poles is possible.



**2. THE UNIQUE ARCHITECTURE** of the AD9026/7 ADCs from Analog Devices targets it at digital baseband RF applications. To gain the high accuracy needed for such applications, it first employs three ADCs—two 5-bit and one 4-bit—to produce a 14-bit conversion. The result is then error-corrected and reduced to 12 bits for increased accuracy.

Low-cost digital base stations also open up the possibility of having wireless PABX services located within buildings or on campuses. The intelligent base station can be programmed to provide a microcell that in turn provides authorized cellular telephones with direct access to intra-campus calls or other PABX services at no charge. Visitors' telephones can automatically have outside calls billed to their home cellular communication system.

Given the ability to directly digitize a 15-MHz portion of the spectrum, one can expect to see a new wave of products in which RF signals will be processed and handled digitally much as audio and video signals are today. Tom Gratzek, ADC product line director for broadband communications at Analog Devices, speculates that digital baseband technology will first find its way into advanced test-and-measurement instrumentation, such as spectrum analyzers, ultrasonic imaging devices, and cellular-system test equipment.

Development of products to digitize video for head-end cable-TV systems also is also under development. As component cost drops, Gratzek anticipates that it will migrate into consumer technologies, such as base stations for European portable telephones that adhere to the DECT (Digital European Cellular Telephones) standard, as well as Japanese telephone sets that meet the personal-handy-phone (PHP) standard. Excited about the possibilities, Gratzek claims that "this technology also positions Analog Devices to meet the future needs of equipment manufacturers for the emerging U.S. personal-communication-system (PCS) infrastructure."

The ADC9026 and ADC9027 are functionally identical except that the ADC9026 has TTL-compatible logic levels while the ADC9027 employs ECL logic levels. Both converter models are packaged in a custom, multilayered, co-fired ceramic DIP along with power-supply bypass capacitors. Each converter model dissipates 1.5 W of power from ±5-V power- supply rails. ☐

## PRICE AND AVAILABILITY

*Both the ADC9026 and ADC9027 ADCs are available immediately in production quantities at $238 each.*

*Analog Devices Inc., 7910 Triad Center Dr., Greensboro, NC 27409-9605; Tom Gratzek, (910) 605-4223.* **CIRCLE 511**

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| MODERATELY | 531 |
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extra traffic capacity within a congested area by creating a micro cell within an existing coverage zone.

The computer-based signal-processing scheme also yields another, unexpected advantage: Using a programmable signal processor means that no hardware changes are required to adapt the system to handle other signal types (such as TDMA, ETDMA, GSM, or even CDMA). A software update can assign a station's channels to select and process analog, digital, or spread-spectrum digital calls on an as-needed basis. Even sophisticated frequency reuse schemes like CDPD messaging may be accommodated by simply installing new software. This means that cellular network operators can easily adapt their digital base stations to changing transmission technologies without expensive "forklift" hardware upgrades.

Contact Russ Cyr at Steinbrecher, 30 North Ave., Burlington, Mass. 01803-3398; (617) 273-1400.

# PRODUCTS NEWSLETTER

## Spice Handbook Comes With Floppy Disk

Since June, 1986, Intusoft, San Pedro, Calif., has been providing free technical information about Spice through a bimonthly newsletter. Now, the company is selling a compilation of all the back issues of that newsletter. *Spice Applications Handbook, 2nd Edition*, contains all of the 34 past issues dating from June, 1986 to January, 1994. There are over 60 technical articles that offer Spice simulation tips and techniques, modeling information, and actual Spice models for a variety of components. Some of the topics discussed in depth include analog behavioral modeling, switched-capacitor models, pressure-sensor models, fuse models, and thermal analysis. A companion disk contains all the models, Spice net lists, and associated schematics and symbols from all of the newsletters. The book and disk are available now for $49.95. Call Intusoft at (310) 833-0710. The company's Internet address is 71564.3147@compuserve.com. *LM* **CIRCLE 597**

## DRAM-Based Graphics Board Handles 64 Bits

The SpeedStar graphics accelerator, which comes in 1- and 2-Mbyte versions, handles 64 bits. The board, from Diamond Computer Systems, Sunnyvale, Calif., speeds Windows and other graphic-intensive applications while displaying true-color graphics and flicker-free refresh rates. The 64-bit connection improves Windows performance for such graphics functions as BitBLTs, raster operations, line drawing, and cursor control. It is built with a Cirrus Logic CL-GD5434 graphics controller, which permits the use of low-cost DRAM. The 2-Mbyte version supplies up to 75-Hz refresh rates with 16.7 million colors at a resolution of 800-by-600 pixels and 256 colors with 1280 by 1024 pixels. Driver support is included for Windows, OS/2, Windows NT, Lotus 1-2-3, AutoCAD, and other popular applications. The Display Power Management Signaling (DPMS) utilities for DOS and Windows, which help reduce the system's power consumption, are integrated into the board. The 1-Mbyte SpeedStar costs $195 and the 2-Mbyte model sells for $235. The 1-Mbyte board can be upgraded to 2 Mbytes for $80. For more information, call the company at (408)736-2000. *RN* **CIRCLE 598**

## Graphics Accelerator Runs At 128 Bits

As 64-bit graphics accelerators are becoming mainstream products, Number Nine Corp., Lexington, Mass., debuted the Imagine-128, a 128-bit graphics and multimedia processor. The chip employs a 128-bit memory controller, which handles the traffic to and from the processor at sustained bandwidths of 500 Mbytes/s. As a result, there is no noticeable performance loss when the system switches from a 16- to a 24-bit color depth. For complex imaging and multimedia applications, the chip supports various drawing primitives and display functions. Up to 16 pixels can be modified in one instruction cycle. Number Nine offers a development kit to simplify integration of the part. The $2495 kit includes a reference board, schematics, a technical reference and programmer's guide, a software development library, a non-line debugger, diagnostics, and related utilities. The Microsoft Windows driver source code is available for $15,000. The chip, which is sampling now, will be in production in the fourth quarter and will sell for $160 in quantities of 10,000. Boards based on the Imagine-128 will be available from Number Nine in the fourth quarter as well. For more information on the Imagine-128 128-bit accelerator, contact the company at (617) 674-0009. *RN* **CIRCLE 599**

## Portable Fax Machine Fits In A Pocket

Measuring just 6.4-by-1.9-by-0.9 in., the 3Fax is a battery-powered fax machine from Psion Inc., Concord, Mass. The tiny device can format documents complete with customized cover sheets, company logos, and signatures. It can also store faxes, defer them to be sent at different times, automatically redial busy numbers, and keep a status log and database of numbers. Users can create the documents using the device's integrated editing system. They also can gain access to E-mail and on-line information services. The 3Fax runs with the Psion's Series 3a machine which is a full-function hand-held computer. The Series 3a contains a large LCD that handles 80 characters and 17 lines of text. The 3Fax, which runs on two AA batteries, sells for $299. For more information, call Psion at (508) 371-0310. *RN* **CIRCLE 600**

*Edited by Clifford Meth*

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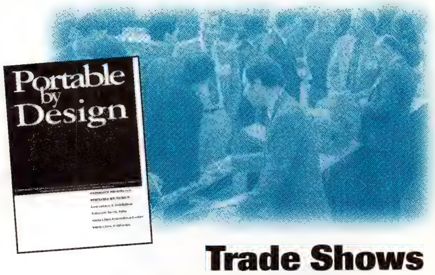

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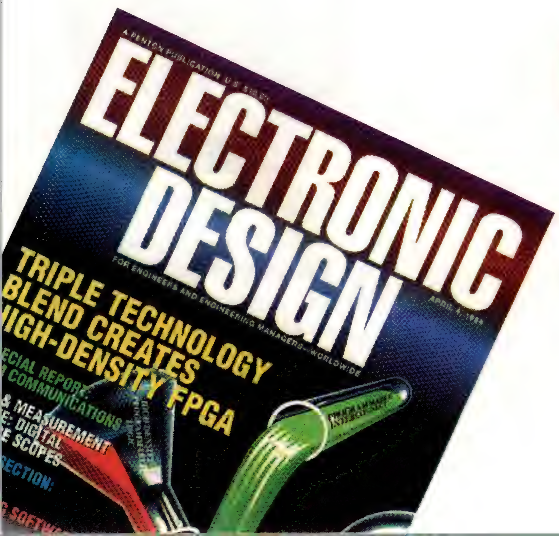

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## DICTATION SYSTEM HOLDS 60,000 ACTIVE WORDS

There's not a large limitation when using version 3.0 of the DragonDictate family of speech-to-text dictation systems—it has a vocabulary of 60,000 active words. With the system, PC users can enter text, control software programs, and operate their computers hands free by speaking rather than typing. This high-end version is intended for users who require extensive vocabularies for dictating widely diverse or specialized subject matter.

The system requires at least a 33-MHz 486-based platform, 8 Mbytes or RAM, DOS 5.0, and 29 Mbytes of free hard-disk space. Costing $1995, DragonDictate is available now. Less powerful versions are also available. A 30,000-word unit is priced at $995, while 5,000-word model sells for $695. RN

***Dragon Systems Inc., 320 Nevada St., Newton, MA 97006; (617) 965-5200.*** CIRCLE 630

## MO DRIVE STORES 230 MBYTES

The MTA-3230 rewritable optical disk drive stores 230 Mbytes of data per cartridge. The magneto-optical (MO) drive is fully compatible with 128-Mbyte cartridges. Its rotational speed of 3600 rpm, a 243-kbyte read-ahead cache, and advanced cache management features combine to offer a data-transfer rate of 1.47 Mbytes/s. The unit contains an auto-write calibration technique that helps optimize the laser power used for writing operations. Available now, the MTA-3230 magneto-optical rewritable disk drive is priced at $700. RN

***IBM Corp., Storage Systems Div., 5600 Cottle Rd., San Jose, CA 95037; (415) 903-0955.*** CIRCLE 631

## VIDEO-EDITOR ADDS TOUCH-SCREEN INTERFACE

The EditStation is a standalone video-editing system with a Microsoft Windows touch-screen user interface. The system also incorporates the powerful media integration capabilities of the IMTX 8000, an audio and video routing and multiple-deck control peripheral.

The EditStation is a complete video post-production system containing two source video tape decks, a recording deck, the IMTX 8000, a Commodore Amiga computer, and two color video monitors. The system is controlled by the user through the Windows-based PC.

A device called the NewTek Toaster is included to add special video effects. Bundled software includes EditWare, which runs under Windows. With EditWare, the user controls all video-editing functions on one screen. Functions controlled by the software include video-clip identification and cataloging, source input and time code striping, video and audio dubbing, edit-list creation and management, and tape duplication. The EditStation is available now. Prices range from $55,000 to $70,000, depending on the chosen video-deck and its format. In addition, hardware and software upgrades are available. RN

***Interactive Media Technologies Inc., 13402 N. Scottsdale Rd., Suite B-155, Scottsdale, AZ 85254; (602) 443-3093.*** CIRCLE 632

## UPGRADE USING WAVE-TABLE SYNTHESIS

An ordinary PC can be transformed into a multimedia entertainment center using the Explorer upgrade system. The system features a sound card that employs wave-table synthesis, a plug-and-play interface card, and a double-speed CD-ROM drive. The Explorer is fully compatible with most industry standards, including Sound Blaster, Windows Sound System, and Ad Lib. It also supports MPEG video on CD, which means that users can play back 74 minutes of full-motion video with an optional MPEG decoder board. Available immediately, the multimedia upgrade system is priced under $500. RN

***Aztech Labs Inc., 46707 Fremont Blvd., Fremont, CA 94538; (510) 623-8988.*** CIRCLE 633

## SOLID-STATE MEMORY CARDS HOLD 40 MBYTES

A family of six PCMCIA-based solid-state memory cards come from the technology alliance between IBM and Toshiba. The cards, sold by IBM, employ Toshiba's high-performance 16-Mbit NAND EEPROMs and an IBM-designed intelligent microcontroller. The result are transfer rates of 7 Mbytes/s on read operations, and 1.2 Mbytes/s on writes. The cards capacities range from 3 to 40 Mbytes. The 3-, 5-, 10-, and 20-Mbyte models fit a Type I form factor, while the 30- and 40-Mbyte models come in a Type II form factor.

The flash architecture stores and retrieves data for an entire sector using parallel read and write operations to increase the transfer rates. The cards' PCMCIA-ATA interface let them act as IDE-based hard-disk drives, making them interchangeable with standard PCMCIA-based rotating memory. In large quantities, the cards sell for less than $25 per Mbyte. RN

***IBM Microelectronics, 1580 Route 52, Internal Zip B, Hopewell Junction, NY 12533; (800) IBM-0181.*** CIRCLE 634

## 12.7-MM-HIGH DISK DRIVE STORES 350 MBYTES

Designed to meet the needs of the shrinking notebook computers, the Filepro Notebook Low Profile 350 (CFL350) 2.5-in. hard-disk drive stores 350 Mbytes of data in a 0.5-in.-high (12.7-mm) form factor. In addition to the small size, the drive weighs just 4.9 oz.

The performance specifications weren't compromised to reached the small size—the drive's average seek time is 12 ms and it supports PIO mode 3 of the enhanced IDE interface for data-transfer rates of up to 11.2 Mbytes/s. A 32-kbyte comes standard and can be increased to 64 kbytes.

Using a series of power-saving techniques, the spindle motor can be shut down during periods of inactivity. In idle mode, with the drive spinning but not reading or writing data, it consumes about 0.75 W. In standby, it consumes just 0.15 W. The drive can withstand an operating shock of 100 Gs and boasts a mean-time between failure rating of 300,000 hours. Single-unit pricing is set at $375. Drives will be available sometime in the third quarter. RN

***Conner Peripherals Inc., 3081 Zanker Rd., San Jose, CA 96134; (408) 456-4500.*** CIRCLE 635

## DUAL OP AMP LINKS PRECISION, SPEED

A dual-current-feedback amplifier, the LM6182 is optimized for high precision and speed. It is ideal for video and other high-speed amplifier applications ranging from Asymmetric Digital Subscriber Lines (ADSL) to imaging equipment. High precision in the LM6182 is achievable through its 3-mV maximum offset voltage, and 5-μA maximum inverting and 2-μA maximum non-inverting input bias current specifications. It features a 100-MHz bandwidth, a 2000-V/μs slew rate, and a 50-ns to 0.1% settling time. In addition, the LM6182 has a 100-mA output current and a high-power output stage, which enables each amplifier to drive a 2-V signal into 50- or 75-Ω back-terminated coaxial cable systems. The LM6812 is fully characterized and specified at both ±5 V and ±15 V, and operates over a temperature range of -25°C to +85°C. It is available in both A- and standard grades, in packages with either 16-pin SO or 8-pin plastic DIP formats. Prices for the A-grade and standard grade, in 1000 unit lots, are $4.30 and $3.60 each, respectively. CA

***National Semiconductor, 2900 Semiconductor Dr., P.O. Box 58090, M.S. 16.300, Santa Clara, CA; Mark Cosgrove, (408) 721-6973.*** CIRCLE 636

## VIDEO ADC FOR PC MULTIMEDIA

The HI1179 IC is a 40 million-sample-per-second (MSPS) 8-bit video a-d converter with an on-chip sync clamp to eliminate several external components normally used for dc restore in desktop multimedia applications. It includes on-chip reference plus sample and hold and dissipates a maximum 110 mW. The HI1179 clamps a portion of the analog input to a reference voltage without a typical external configuration of six resistors, a potentiometer, a sample-and-hold circuit, and an op amp. This centers an ac-coupled waveform within the a-d converter's range of maximum accuracy. Ac-coupled video signals require dc restore before the a-d conversion stage. Clamping is used in video circuits where the video signal is on one side of a reference baseline and horizontal and vertical synchronizing (sync) signals are on the other. This maintains the video signal at a reference baseline level. The on-chip voltage reference sets the analog input range for 0.6 to 2.6 V. External references can range between 0 and 2.8 V.

The HI1179's typical 40 MSPS conversion rate (35 MSPS minimum guaranteed) allows eight-times oversampling of 3.58 MHz NTSC plus 4.43 MHz PAL and SECAM color subcarrier frequencies. Applications include PC multimedia, desktop video editing, TV production equipment, digital scanners, hand-held test equipment, and high-speed data acquisition systems. Effective DSP requires converters that can oversample the Nyquist criterion. Oversampling reduces the performance requirements for the anti-aliasing filter used ahead of the data converter, which in turn simplifies front-end design and lowers system cost. In addition, oversampling helps accommodate limitations such as aperture jitter in other parts of the system. The HI1179 comes in 32-lead plastic quad flatpacks. In lots of 1000, it costs $10.16. CM

***Harris Semiconductors, P.O. Box 883, Melbourne, Fla. 32901; (800)-4-HARRIS.*** CIRCLE 637

## 12-BIT DACS FEATURE DIP AND SO PACKAGES

Two industry-standard monolithic 12-bit d-a converters, the MX565A/566A have been optimized for speed and packaging. Suitable for such applications as CRT drivers and fast a-d converters, the MX565A offers a 10-V, 10-ppm/deg C precision reference, while the MX566A utilizes an external reference. In addition, both DACs have fast settling times—both settle to within ±1/2 LSB in a maximum of 250 ns, (the MX566A requires 350 ns maximum). In addition, the MX565A has an accuracy with respect to full scale of 1/4 LSB maximum, with monotonicity and ±1/2 LSB accuracy guaranteed over the temperature range of 0°C to 70°C (commercial) for both DACs. The MX565A is powered by a ±15-V supply; the MX566A requires -15 V. Both the MX565A and the MX566A are available in a 24-pin plastic DIP, ceramic DIP, or SO package. In lots of 1000, they cost $9.68 and $9.04 each, respectively. CA

***Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA, 94086; (408) 737-7600, ext. 6087.*** CIRCLE 638

## OPTOELECTRONIC ICS BOAST LOW COST

The OPT202 and OPT209 low-cost, high-performance optoelectronic ICs are targeted at precision instrumentation, scanning, and sensing applications. The monolithic ICs integrate a large 0.09-by-0.09-in. photodiode, precision FET-input transimpedance amplifier and a 1-MΩ feedback resistor on a single chip.

Photodiode current is converted to an output voltage proportional to the light's intensity. The OPT209's bandwidth is 16 kHz, providing excellent performance for general-purpose applications. The OPT202's bandwidth is 50 kHz, which is ideal for pulsed-light applications, such as barcode scanners.

The OPT202 and OPT209's precision, versatility, and low cost make them ideal for industrial applications, including medical and laboratory instrumentation, position and proximity sensors, photographic analyzers, and smoke detectors. Their combination of photodiode and amplifier eliminates many problems commonly associated with discrete designs, such as leakage-current errors, noise pick-up, and gain peaking due to stray capacitance. Photodiode responsivity is 0.45 A/W at 650 nm.

Key specifications for the ICs include: 2-mV dark errors, 400-μA quiescent current, 0.05% nonlinearity, and ±2.25 to ±18 V supply range. Specified over the commercial temperature range of 0°C to +70°C, the OPT202 and OPT209 are packaged in clear plastic 8-pin DIPs. Dice are also available. The OPT202 starts at $4.25 in lots of 1000; the OPT209 costs $5.25. Delivery is from stock.

***Burr-Brown Corp.,*** *P.O. Box 11400, Tuscon, Arizona 85734; (800) 548-6132.* CIRCLE 639

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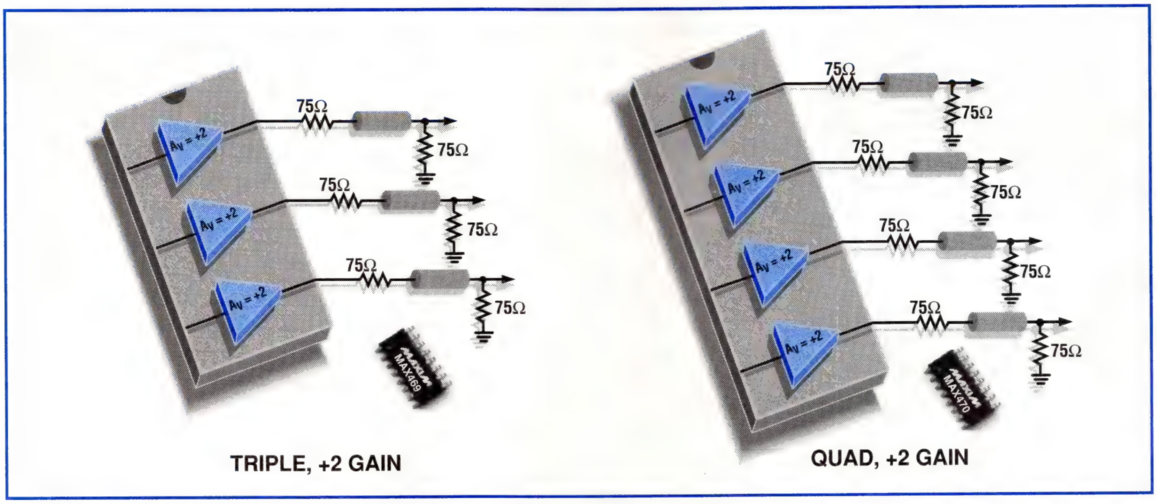

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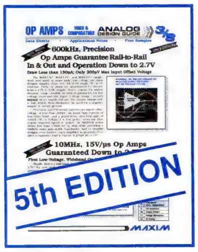
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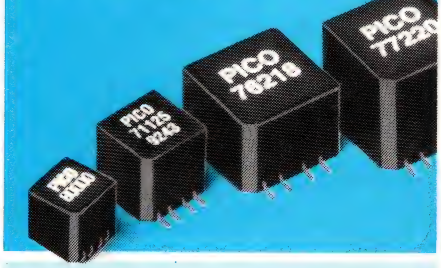

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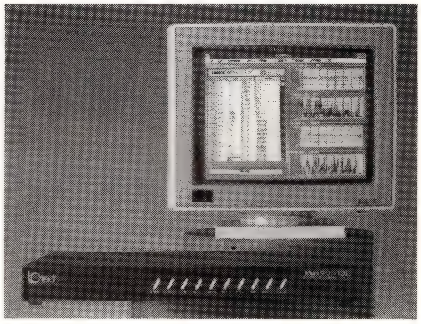
# TEMPERATURE/VOLTAGE UNIT SCANS 147 CHANNELS/S

The MultiScan/1200 temperature and voltage measurement instrument scans up to 147 channels/s or digitizes waveforms at up to 20 kHz. As a 19-rack-mountable unit, the instrument offers channel-to-channel isolation not found in PC plug-in boards and the accuracy of more expensive, but slower, data loggers.

The system accepts up to 24 differential inputs in any combination of voltage and temperature. A 16-bit analog-to-digital converter, oversampling, and averaging ensure low noise and ac line rejection. Using Exp/10A expansion modules, a maximum of 744 channels are possible. Two scanning modules are currently available for the MultiScan/1200. The MTC/24 thermocouple/volts module supplies 24 differential input channels with per-channel programmability. The MHV/24 high-voltage module has 24 differential voltage-input channels with per-channel programmability for up to ±250 V full-scan. Both unit provide 250-V peak dc isolation.



Included with the MultiScan/1200 is MultiView, a Windows application that allows users to graphically configure channel characteristics and scanning requirements. It also offers several options for viewing, plotting, and saving measurement data. Another included Windows application, PostView, lets users graphically scroll through data files previously acquired with MultiView. It allows simultaneous display of 32 channels, with independent cursors for each.

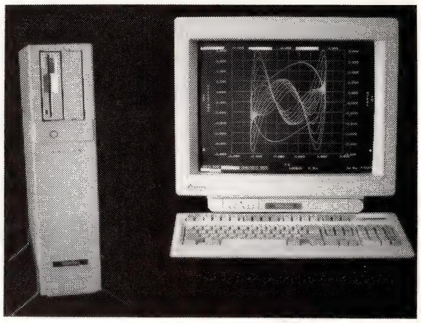
The MultiScan/1200 costs $1495. The MTC/24 and MHV/24 scanning modules and the Exp/10A expansion module each cost $995. Delivery is in four to six weeks.

*IOtech Inc., 25971 Cannon Rd., Cleveland, OH 44146; (216) 439-4091.* **CIRCLE 640**

■ *JOHN NOVELLINO*

## SYSTEM ACQUIRES, LOGS DATA ON 32 CHANNELS

The Visidaq Model 3200 is a data visualization/acquisition system that supplies up to 32 channels of high-speed, 12-bit data logging. For ease of use, the system is menu-driven and employs single-key options for all setup and operational tasks. Maximum sampling rate is 178,000 samples/s on one channel, and 1000 samples/s each on 16 channels. Users can select strip chart, xy, or numeric page display to acquire, log, display, annotate, playback, analyze, reduce, store, or print any sensor data recorded. Also, the Model 3200 can be used as a file server to distribute the acquired data enterprise wide without tying up the test stand. The system provides MS-DOS formatting and uses a Posix-compliant Unix operating system that allows the 3200 to function as an X-Window workstation. Available functions include signal rearrangement, engineering unit scaling, delta calculations, data searches, statistics, multiple display formats, limit alarms, and data reduction. Model 3200 prices start at $29,990. Delivery is in 30 days. JN



***Visidaq Solutions Inc., 1970 Swarthmore Ave., Lakewood Industrial Park No. 3, Lakewood, NJ 08701; (908) 901-6100.*** **CIRCLE 641**

# NO SUBHARMONIC NOISE! 94% EFFICIENT DC-DC STEP-DOWNS POWER WIRELESS SYSTEMS

## Internal Switches and Surface-Mount Packages Save Space

Compact size, battery-saving features, and low-noise make this new family of pulse-width modulated (PWM) step-down DC-DC converters ideal for portable communications and wireless applications. These drop-in replacements for Maxim's popular MAX730-family deliver up to 50% more output current, are free of subharmonic switching noise, maintain up to 94% efficiency, and are lower priced. And, the MAX744A has guaranteed 159kHz to 212.5kHz oscillator limits to avoid interference in the sensitive 455kHz IF band. External component selection has already been optimized to simplify design work.

- **No Subharmonic Switching Noise with Low $V_{IN}$-$V_{OUT}$ Differentials**
- **88% - 94% Efficiency**
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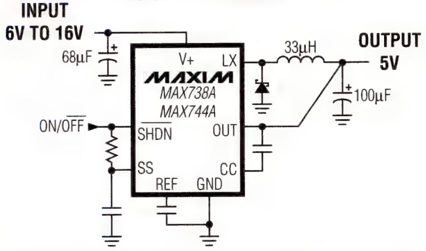
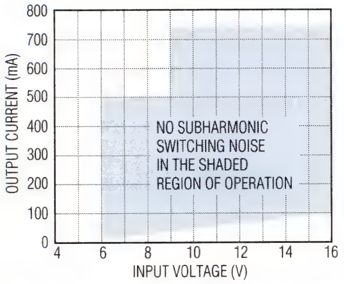
- **Up to 750mA Output Currents, Guaranteed**
- **Logic-Controlled 6µA Shutdown**
- **5V, 3.3V, or Adjustable Outputs (1.25V to $V_{IN}$)**
- **Evaluation Kits Available†**

| DEVICE | REPLACES | OUTPUT VOLTAGE | INPUT RANGE | PRICE* |
|---|---|---|---|---|
| MAX730A | MAX730 | 5V | 5.2V–11V | $2.15 |
| MAX738A | MAX738 | 5V | 6V–16V | $2.60 |
| MAX744A | NEW | 5V | 6V–16V | $2.90 |
| MAX748A | NEW | 3.3V | 3.3V–16V | $2.60 |
| MAX763A | NEW | 3.3V | 3.3V–11V | $2.15 |
| MAX750A | MAX750 | ADJ | 4V–16V | $2.15 |
| MAX758A | MAX758 | ADJ | 4V–11V | $2.60 |

**LOW-NOISE, COMPACT STEP-DOWN IS 94% EFFICIENT**

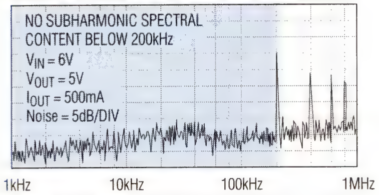


**NO SUBHARMONIC NOISE OVER WIDE OPERATING RANGE**

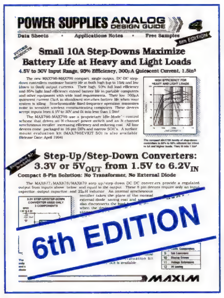


*The MAX744A exhibits no subharmonic switching noise over a wide input voltage and output current range.*

**SPECTRAL ANALYSIS OF MAX744A OUTPUT VOLTAGE NOISE vs. FREQUENCY**



*The MAX744A output voltage noise spectra shows no switching noise below the 200kHz fundamental switching frequency.*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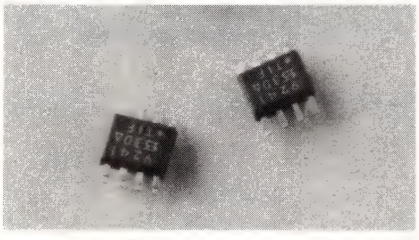
† Order MAX738EVKIT-DIP or MAX738EVKIT-SO and appropriate free sample.

# SMALL-OUTLINE BUS DRIVERS SUIT AUTOMOTIVE DIAGNOSTICS



Now that the ISO 9141 standard for communication between automotive computers and diagnostic equipment is beginning to take hold in the U.S., designers will need a means of facilitating that communication. The Si9241EY and Si9243EY compact, single-ended bus drivers from Siliconix are claimed as the first narrow-body, small-outline devices to meet that standard.

The Si924X Series enables communication over the relatively long distances between test equipment and automotive electronic control units, while protecting sensitive logic devices from the hazards of the automotive environment. These protection features include short-circuit and overvoltage protection. In addition, the devices' rugged design ensures that they can handle the high voltages and stresses imposed by such conditions as load dumps, field decay, and other automotive transients.

Used either in the automobile itself or in the external test equipment, the drivers will replace up to 20 discrete devices with a single SO-8 package. Two options are offered to suit different ISO 9141 configurations, the Si9241EY and the Si9243EY. The Si9241EY driver provides communication capability over the bidirectional K line and a pinout for fault-detection circuitry. The Si9243EY provides both K and L line pinouts. There's no pinout on the 8-pin device for the fault-detection circuitry, but this feature remains active as in the Si9241EY.

Samples of both drivers are available now with production-quantity lead times of stock to eight weeks. In large lots, pricing is $0.89 for the Si9241EY and $1.05 for the Si9243EY.

***Siliconix,*** *2201 Laurelwood Rd., P.O. Box 54951, Santa Clara, CA 95056-0951; (800) 554-5565, ext. 29.* CIRCLE 642

■ *DAVID MALINIAK*

# DIGITAL VIDEO PROCESSOR HANDLES REAL-TIME IMAGES

Supplying a cost-effective bridge between computer graphics and video images, the CL-Px1070 is built with internal FIFO buffers and pipelined processing to allow conversion between standards that had been previously incompatible. The part suits end products that require real-time digital video processing, such as low-cost teleconferencing systems, video-playback acceleration, and video capture. Like its predecessor, the Px2070, the Px1070 allows overlaying video on graphics or vice versa in real time. It also performs scaling, zooming, color-space separation, and video-graphics genlocking.

The digital video processor (DVP) combines real-time video scaling with frame-buffer memory management, a programmable host-system-bus interface, and a flexible multistream video data path. Its versatile windowing control allows resizing and moving the video display window with no host-bandwidth penalty. The DVP supplies four I/O ports that can connect directly to multiple independent I/O devices, including the host. Two ports can receive video from almost any type of source. The third connects to the host through an ISA or Micro Channel bus; the fourth is attached to a video-memory buffer. The Px1070 is available now for $26 in large quantities.

***Cirrus Logic Inc.,*** *3100 West Warren Ave., Fremont, CA 94538; (510) 623-8300.* CIRCLE 643

■ *RICHARD NASS*

# MPEG I DECODER EASES MULTIMEDIA CARD DESIGN

In addition to performing full-motion-video decompression according to the MPEG I standard, the ZR36100 is the first MPEG I decoder to process the MPEG I system-layer information. That processing includes separating the discrete MPEG I video and audio bit streams and automatically synchronizing the decompressed video output with the output data of a downstream MPEG I audio chip.

The ZR36100 MPEG I decoder eliminates a considerable amount of system overhead logic, including the need for a host processor or dedicated microcontroller. That will further reduce the cost of adding MPEG I decompression to computer systems.

The CMOS chip fully conforms to the MPEG I standard, processing MPEG bit streams at rates of up to 5 Mbits/s. That allows the chip to support SIF resolutions for both 352-by-240-pixel NTSC (30 Hz), and 352-by-288-pixel PAL (25 Hz) formats. Features of the chip include user-selectable progressive or full CCIR601 interlaced video output, as well as special commands for 3:2 pull down, random access, fast search, slow motion, single stepping, and freeze-frame. In addition, the ZR36100 can do high-resolution still-image decoding.

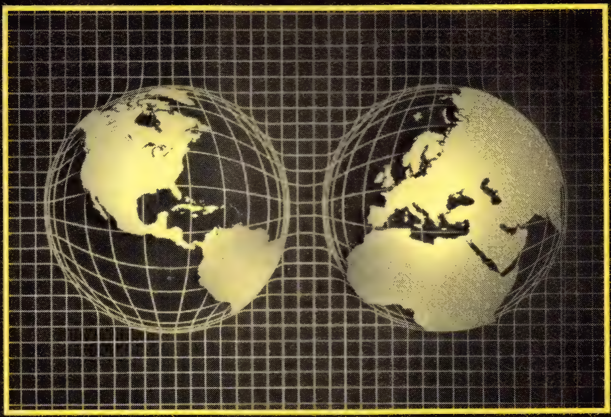
The combination of features positions the chip well for cost-sensitive multimedia subsystems. As lower-cost systems proliferate, MPEG I playback will be adopted as a standard system feature, putting it in the mainstream, rather than relegating it to an optional function.

Housed in a 128-lead quad-sided flat package, the ZR36100 is immediately available and sells for $30 each in large quantities. An evaluation board is also available and sells for $1995.

***Zoran Corp.,*** *1705 Wyatt Dr., Santa Clara, CA 95054; Abbas Razavi, (408) 986-1314.* CIRCLE 644

■ *DAVE BURSKY*

# Technology on the Move



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READER SERVICE 132

# CACHE CONTROLLER RUNS MULTIPLE PENTIUMS

Enhancing the uniprocessor cache controller it released last year for Intel's Pentium CPU, designers at Vitesse Semiconductor have crafted a multiprocessor version that can support symmetric multiprocessor systems. The VSP947 multiprocessor cache controller and companion VSP948 datapath circuit are used in conjunction with a new multiprocessing bus architecture—the V-Bus—to form SMP systems. Those systems can scale linearly, able to support up to 12 Pentium CPUs while maintaining zero-wait-state performance. In addition, the chip set can work with either the 3- or 5-V versions of the Pentium that run at bus speeds of 60 or 66 MHz (90 and 100 MHz, internally), with a migration path to bus speeds of 80 MHz.

The V-Bus is a 66-MHz split-transaction bus that supports a sustained bandwidth of 500 Mbytes/s and on-the-fly error correction. The cache controller handles cache sizes from 512 kbytes up to 8 Mbytes. Incorporated in the chip set is an eight-level write-back buffer to reduce bus traffic, as well as a trio of other buffers—one for posted writes, another for line fills, and the third for a snoop line. All of the buffers help system performance by improving the parallelism of system operations. These buffers combine with zero-wait-state snoop support to enable 1-1-1-1 pipelined and 2-1-1-1 non-pipelined CPU reads and writes. Furthermore, the cache chip set handles both direct-mapped and two-way set associative protocols. The MESI protocol is also supported to ensure data consistency.

The VSP947 comes in a 292-contact ball-grid array package and is implemented with Vitesse's H-GaAs III gallium-arsenide process, while the datapath chip is implemented in CMOS and is housed in a 208-lead PQFP. The high speed of the VSP947 allows system designers to use standard asynchronous static RAMs for tag entries and standard burst SRAMs for data storage. The datapath chip provides control for data and parity on the processor bus. In addition, it buffers the datapath between the system and the processor. The first systems to incorporate the chip set will be released later this year by Tricord Systems Inc., Minneapolis, Minn.

In lots of 1000 sets, the VSP947/948 chip set sells for $250. apiece. Samples will be ready in the late third quarter.

***Vitesse Semiconductor Corp.,*** *741 Calle Plano, Camarillo, CA 93012; Brett Butler, (805) 388-3700.* **CIRCLE 645**

■ *DAVE BURSKY*

## PROGRAMMABLE CHIP AIDS PC JOYSTICKS

A CMOS programmable chip, the EZ1000 is specifically optimized for use in input devices, such as joysticks and game pads. It offers intuitive control functionality, low power consumption, and high performance at a low cost. The chip features 2K of on-chip memory and an 8-input programmable controller. In addition, the chip has a clock speed of 4 MHz, with a 1-$\mu$s instruction cycle, and is powered by the pc power line in a keyboard, (nominal 5-V supply). Its high-performance design allows for the execution of a command in a single action, a feat which previously required several keyboard strokes. Available in a 28-pin package, the EZ1000 costs $10 each. CA

***Rosetta Technologies, 1310 RR 620 South, Suite B195, Austin, TX; Israel Martinez, (512) 263-1700.*** **CIRCLE 646**

## CHIPS DECODE ANALOG VIDEO, ENCODE DIGITAL

With the ability to create the digital video signals needed by a computer, the CL-Px4070 TV-In decoder can translate the analog signal output of a television camera or VCR and convert it into the digital signals needed by an RGB computer display. The CL-Px4080 Video-Out encoder, bridges the gap between the analog TV/video standards and the desktop computers's digital video standard. Together, the two chips provide a solution for merging the computer and the television. The CL-Px4070 combines the functions of a video digitizer and video decoder in one chip—it accepts NTSC, PAL or SECAM broadcast signals and converts the signal stream into the digital YUV format used by the computer. The chip's 16-bit output can be connected to a video processor, such as the company's CL-Px2070 or PX1070. The 4080 is a multistandard encoder that basically reverses the process to display the video image on a television or VCR. Samples of both chips are immediately available and sell for $21 and $15, each, in lots of 50,000. DB

***Cirrus Logic Inc., 3100 West Warren Ave., Fremont, CA 94538; Gerald Wineinger, (214) 985-2340.*** **CIRCLE 641**

## LOW-COST ASIC PUSHES 1200 DOTS/IN.

A new generation of printer controller and software technology supplies the impetus for the development of low-cost Windows-based printers. Such printers can handle a resolution of 1200 dots/in. and offer simultaneous support of PC and Macintosh platforms. Other features of the WinStyler ASIC include bidirection communication and the ability to produce virtually any document at the rated engine speed.

The WinStyler's host-based printing concept relies on a combination of a lean printer controller that includes the ASIC, the host-based printer software, either a serial or parallel interface, and the processing power of the host. The result is accelerated printer output and reduced printer manufacturing costs due to the elimination of an expensive CPU and a reduced memory requirement. The controller is capable of rasterizing and sending the high-resolution images form the host computer to the printer at speeds commonly associated with less sophisticated 300-dot/in. printers. RN

***Destiny Technology Corp., 3255-1 Scott Blvd., Suite 201, Santa Clara, CA 95054; (408) 562-1000.*** **CIRCLE 648**

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**READER SERVICE 121**

## TV TO COMPUTER DISPLAY WITH ONE CARD

With the implementation of Simply TV, a single-color graphics card, any television can be quickly and easily turned into a large-screen Macintosh display. Simply TV, designed for easy installation connects any Macintosh LC, Color Classic, most Performa models, and the Quadra 605, to a television via a single video cable. The TV, which is now an inexpensive large-screen display, can then be used in a variety of applications for viewing such things as CD-ROM's, educational software, and corporate video presentations. Simply TV features built-in chroma-lock technology, to digitally lock colors in place, and hardware-based convolution technology, to aid in the elimination of flicker. In addition, the card comes equipped with S-video capability. Simply-TV is costs $439. CA

***E-Machines, 215 Moffett Park Dr., Sunnyvale, CA, 94089; Eric Zetlin, (408) 541-5393.*** **CIRCLE 649**

## BOARD IS COMPATIBLE WITH SPARCSTATION 5

Based on the microSparc II microprocessor, the Sparc CPU-5CE 6U VMEbus board is compatible with the SparcStation 5 workstation. Backward compatible with the company's previous products, the CPU-5CE performs over 64 SPECint92 and 85 MIPS. These numbers are due to the high-performance processor, which integrates the integer and floating-point units with the memory-management unit, 16 kbytes of instruction cache, 8 kbytes of data cache, memory control, and an SBus interface.

The board can hold up to 64 Mbytes of DRAM. Interfaces are included for fast SCSI-2, Ethernet, a floppy-disk drive, parallel and serial I/O, and a mouse and keyboard. Two SBus modules fit on the board, enabling further expansion. Solaris 1.1 and 2.3 are both available. For real-time applications, VxWorks has been ported to the CPU-5CE. With 16 Mbytes of memory, the CPU-5CE costs $4995. A higher-performance model will be released shortly. RN

***Force Computers Inc., 2001 Logic Dr., San Jose, CA 95124; (408) 371-5900.*** **CIRCLE 650**

## FLASH DISK EMULATES HARD-DISK DRIVE

The solid-state PC Flash Disk is essentially a hard-disk drive with no moving parts. Because the drive is based on non-volatile flash memory, it can plug directly into an 8-bit ISA or 16-bit EISA bus slot and replace both the primary disk drive and its associated controller without any additional software or cabling. Its performance is faster than magnetic hard disks while consuming less power. In addition, the drive supplies cold boot and full hard-disk emulation capabilities. Designed for rugged applications, the PC Flash Disk can operate reliably under severe shock, humidity, dust, and temperature conditions. The disk is available in capacities from 1 to 32 Mbytes, and can be expanded to 128 Mbytes by connecting four boards together. On-board BIOS eliminates the need for any installation software. The disk is compatible with MS-DOS, PC-DOS, and Windows. File operations can be performed from any local or remote source to the PC Flash Disk using standard DOS commands. Available now, prices start at $139 in lots of 100. RN

***M-Systems Flash Disk Pioneers Ltd., 556 Mowry Ave., Fremont, CA 94536; (510) 505-9081.*** **CIRCLE 651**

## TINY SBC RUNS AT 100 MHZ

The Little Board computer, which places the equivalent of a PC/AT motherboard plus four expansion cards into the space of a half-height 5-1/4-in. disk drive, has a new member: The Little Board/486 DX4 runs at 100 MHz and includes controllers for serial, parallel, speaker, floppy, IDE hard disk, and SCSI interfaces. There's also room for up to 16 Mbytes of memory and sockets for 32 kbytes of cache and a watchdog timer. Embedded-system reliability is increased by the use of a 1.5-Mbyte bootable solid-state disk. This disk can be EPROM, flash EPROM, or static RAM.

Like other members of the family, the 100-MHz unit accepts industry-standard PC/104 modules for expansion. A host of PC/104 modules are available from many third-party vendors. The operating temperature for the board is 0 to 70°C and the power consumption typically ranges from 5 to 12 W, with +5-V-only operation. Little Board/486 DX4 evaluation units are available now. Large-quantity prices are set at $1950. RN

***Ampro Computers Inc., 990 Almanor Ave., Sunnyvale, CA 94086; (408) 522-2100.*** **CIRCLE 652**

## 14-COLOR LCD ENHANCES INDUSTRIAL COMPUTER

A large color VGA flat-panel display accompanies the industrial computer in the DisplayPac-Vista. The complete workstation is built with a 14-in. color TFT LCD, a 66-MHz 486DX microprocessor, a resistive touch screen, and up to 32 MBytes of DRAM. The system suits space-conscious machine-control and process environments. The entire unit draws about half the power of a comparably sized CRT alone. It's available in a 12.5-by-15.5-by 4.5-in. rugged metal open-frame panel mount, or a 19-in. rack-mount version. Both have bays available for a 1.44-Mbyte floppy drive, a 2.5-in. hard drive (with a capacity up to 500 Mbytes), or a dual-slot PCMCIA socket. In addition, six expansion slots accept standard AT-bus add-in boards. A 33-MHz DisplayPac-Vista system with 4 Mbytes of DRAM starts at $7435. RN

***Computer Dynamics Sales, 107 S. Main St., Greer, SC 29650; (803) 877-8700.*** **CIRCLE 653**

## ACCELERATOR CONNECTS TO SPARC WORKSTATIONS

The SkyStation II multiprocessor desktop accelerator is now available for Sparc-based workstation. The 640-MFLOPS system is suited for the development of floating-point-intensive applications. Using a SCSI-2 connection, it plugs directly into workstations that are running the Solaris operating system. The SkyStation II can be used as a development station in conjunction with VME-based products or as a complete desktop solution when paired with a workstation. Prices range from $20,000 to $50,000 depending on volume and configuration. RN

***Sky Computers Inc., 27 Industrial Ave., Chelmsford, MA 01824; (508) 250-1920.*** **CIRCLE 654**

### TOOLKIT WORKS WITH ALPHA/WINDOWS NT

The MKS Toolkit 4.2 for Digital Equipment's Alpha AXP version of Windows NT includes development utilities for DOS, OS/2, Windows NT, and Digital's Alpha AXP version of NT. Included are tools for command editing and history, file processing and comparison, and text manipulation and sorting. The Windows NT release of the toolkit includes the MKS Vi full-screen editor and MKS Make software construction tools. The MKS Toolkit supplies utilities for the PC usually found only on Unix systems to give all operating platforms the same look and feel. More than 190 commands and utilities are included for customizing an environment and performing a variety of computing tasks. List price of the toolkit for the Alpha version of NT is $299. SVT

***MKS (Mortice Kern Systems), 35 King St. North, Waterloo, Ontario, Canada N2J 2W9; (519) 884-2251; fax -8861.*** CIRCLE 655

### SOFTWARE SIMULATES 386EX PROCESSOR

With the SoftProbe 386EX/SIM Simulator/Debugger, engineers can develop and debug applications for Intel's 386EX embedded processors. The simulator is a DOS-hosted device that supplies bus and instruction-level simulation and affords debugging of real- and protected-mode C/C++ and PL/M applications for the 386EX processor. The simulator is compatible with popular compilers and linkers, including MetaWare's High C/C++ 32-bit optimizing compiler and Microsoft C/C++ optimizing Compiler. Contact the company for pricing. SVT

***Systems & Software Inc. (SSI), 18012 Cowan, Suite 100, Irvine, CA 92714-6809; (714) 833-1700; fax -1900.*** CIRCLE 656

### CM PROGRAM RUNS UNDER WINDOWS

Version 6.2 of MKS RCS configuration management software for DOS/Windows has complete project management facilities, an automatic building process, file promotion, hooks into Visual Basic, and Netware-specific functionality. MKS RCS has a documented API to enable seamless integration into other applications. Integrated project management facilities enable the end user to create and manage projects, using the software's features on individual files within the project or on the entire project at once. It automatically tracks files, revisions of archive files, file changes since the last build, and archive files locked for editing. It also tracks dependencies between files and automatically converts these dependencies to a *make* file. List price is $389; upgrades are $149. SVT

***MKS (Mortice Kern Systems Inc.), 35 King St., Waterloo, Ontario, Canada N2J 2W9; (519) 884-2251; fax -8861.*** CIRCLE 657

### TOOLS OFFER 'PICTURE' SOURCE-CODE DEBUGGING

A data debugging toolset offers a solution to the problem of debugging with complex data-manipulation software. The toolset, now available for Sun workstations, Motorola 167, and CSPI i860 Supercards, was developed to fill a gap between standard source code debuggers and generic graphic toolsets. It supplies non-graphic, logic-based debugging controls to be embedded in a user program under development. The toolset routines generate remote X11 graphic displays, with which the user can view program data results on a Sparc Unix host, control debugging flow, and analyze massive data arrays in a graphical form. Priced at $499 per library, the toolset will run soon on IBM, DEC, HP, and Silicon Graphics workstations. SVT

***CST Images, 5055 Viewridge Ave., San Diego, CA 92123; (619) 277-7833; fax -576-0859; contact Ron Townsen.*** CIRCLE 658

### SOFTWARE DOES MPEG ENCODING FOR CD-ROM

XingCD 1.0 CD-ROM MPEG encoder software for Windows produces MPEG video streams from TGA, AVI, or BMP files. The software also creates MPEG audio streams from WAV files and interleaves audio and video into an MPEG-compatible system steam. It creates full-screen MPEG video streams from various source files, including video captured with AVI-compliant motion JPEG boards, 3D animations, and image files. List price is $995. SVT

***Xing Technology Corp., 1540 W. Branch St., Arroyo Grande, CA 93420; (805) 473-0145; fax -0147.*** CIRCLE 659

### SDK HELPS INTEGRATE TEXT-TO-SPEECH

The TTS (text-to-speech) software-development kit (SDK) helps application developers integrate text-to-speech capabilities into their Windows-based products. The software converts common computer ASCII text, such as data from word-processing documents, spreadsheets, and databases into natural-sounding speech output. Versions are available for English, German, French, and Spanish. The kit includes evaluation software, sample programs, an API function reference and programming guide, and a dynamic-link library with its own data and sample text files. The TTS development kit sells for $1999. The price includes a license fee for one copy of the software in one language. Additional languages are $499. RN

***Lernout & Hauspie Speech Products Inc., 800 West Cummings Park, Suite 3100, Woburn, MA 01801; (617) 932-4118.*** CIRCLE 660

### VERSION SOFTWARE SUPPORTS WORKGROUPS

Versions 1.1 version-control software for Windows manages versions by streamlining management of multiple project resources, including source code, documentation, and other files. The upgrade supplies foolproof work group support, enabling network users to collaborate on projects. Versions 1.1 supports all file types, including binary, so that users can collaborate on source code, resource files, engineering drawings, word-processing documents, spreadsheets, and graphics files. Network-compatible, the program supports multiple developers working on the same project, with storage of temporary and permanent versions of any file. List price is $279. SVT

***StarBase Corp., 18872 MacArthur Blvd., Suite 400, Irvine, CA 92715; (714) 442-4400; fax (714) 253-6712.*** CIRCLE 661

## SONET/ATM TRANSCEIVER SUPPORTS STS-1/3

Physical layer interface design for Sonet/ATM systems is now simplified by the advanced features offered by the CY7B951 Sonet/SDH Serial Transceiver (SST). The chip's dual-frequency feature provides a single-chip PHY-layer interface for data both at STS-1 (51.84 MBits/s) and STS-3/STM-1 (155.52 Mbits/s) data rates. The SST's on-chip 8X clock-multiplier provides very low-jitter clock recovery from NRZ and NRZI data using an inexpensive 19.44-MHz crystal without any external PLL filter capacitors.

Compatible with both the PMC 5345 SUNI and IgT WAC013A ATM framers, the transceiver chip's link-fault sensing circuitry provides a positive indication of signal loss and can automatically switch the SST to internal clock synthesis, preventing receiver PLL run-away. With the selectable loop-back mode, engineers can easily provide in-system diagnostic capability for equipment incorporating this transceiver.

The chip is implemented in low-power biCMOS technology, which allows it to draw less than 50 ma from it's one 5-V supply—less than half of similar bipolar products. The ATM-oriented SST compliments Cypress's recently introduced HOTLink high-speed serial transceiver chipset which is designed primarily for Fibre Channel and ESCON applications.

Both SST and HOTLink are targeted at OEM products such as adapter cards, hubs, routers, and set-top boxes. SST is priced at $45 in lots of 100. LG

***Cypress Semiconductor, 3901 North First Street, San Jose, CA 95134; (408) 943-2600.***

**CIRCLE 662**

## SBUS ATM CARD INCLUDES API BUNDLE

A complete ATM hardware/software solution has arrived at the desktop with the introduction of the ENI-155 family of network interface cards and bundled applications program interface (API) software. The ENI-155 is first card in the series and will provide a 155-MBits/s SONET/SDH link for SBus-based computers over multimode fiber, or Cat 5 UTP copper.

Based on ENI's proprietary Midway ATM processor chip, the cards and software have been optimized for maximum efficiency in the SBus environment.

Included with the cards is a suite of software, which offers complete UNI 3.0 compliant support for the Solaris 2.3 and SunOS 4.1.3 operating systems. The ENI-155 cards will begin shipping in he third quarter of 1994.

The second phase of ENI's releases will be the ENI-155p and 155g, 155-MBits/s ATM adapters designed for PCIBus and GIO bus (Silicon Graphics) computers. The bundled software will include drivers to support Windows NT (NDIS 3.0) and Novel Netware (ODI) for the 155p, and IRX 5.1/2 for the 155g. Delivery is anticipated for the fourth quarter of 1994. Prices of all three boards will be under $1000 in OEM quantities, including software. LG

***Efficient Networks Incorporated., 4201 Spring Valley Road., Suite 1200, Dallas, TX 75244-3666; David Massey, (214) 991-3881.***

**CIRCLE 663**

## SBUS OFFERS 12-TERMINAL CONNECTIVITY

A low-cost SBus terminal server, the LC 12 Sp, is designed to connect up to 12 terminals to Sun computer systems. Equipped with 12 asynchronous serial ports, the LC 12 Sp can connect to any RS-232 device that uses a three-wire connection.

The server features a fully automatic XON/XOFF flow control logic, a data word size ranging from 5 to 8 bits with data transfer rates of up to 115.2 kbits/s, and a 10 MIPS serial processor. The LC 12 Sp driver supports Solaris 1.x, Solaris 2.x, and SunOS 4.1+ software packages. It is fully compatible with Sun Microsystem's SPARC computers and other computers compliant with the SPARC International SBus specification.

Available now, the LC 12 Sp costs $595. Future software updates will be provided at no additional charge. CA

***Magma, 6725 Mesa Ridge Rd., San Diego, CA, 92121; Michael Seidel, (619) 457-0750.*** **CIRCLE 664**

## VOICE/FAX CARD BOASTS HIGH DENSITY

The universal port card, TR118, with eight channels (each powered by a dedicated digital signal processor), is ideal for designers building high-performance, high-volume applications. With its high density levels, the TR118 can handle large enhanced fax and voice systems.

Each of its eight channels, with user-defined functionality, has 1 Mbyte of RAM and can simultaneously send and receive faxes or voice messages. The TR118 card is configured with both MVIP and PEB digital interfaces. In addition, it uses the Applications Programming Interface (API), a "c" language library of call functions that simplifies development of applications, and is supported by UNIX, QNX, OS/2, and DOS systems. The TR118 is available immediately and carries a price tag of $5495. CA

***Brooktrout Technology Incorporated, 144 Gould Street, Needham, MA, 02194; Andrew O'Brien, (617) 449-4100.***

**CIRCLE 665**

## FIBRE CHANNEL TRANSMITTER, RECEIVER

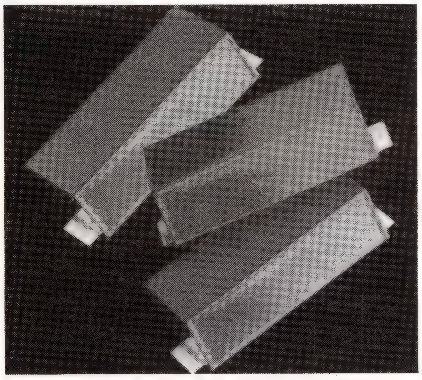
A two-chip Fibre Channel transceiver will give products a low-cost gigabit data link between computers or other peripherals. The HDMP-1512 transmitter and HDMP-1514 receiver can transport data at either 531.25 Mbits/s or 1062.5 Mbits/s and provide complete FC-0 functionality. The transmitter requires 8B/10B encoded data, or equivalent, and a 53.125-MHz clock. The receiver accepts a serial data stream and provides a 20-bit wide parallel output at TTL levels.

Both chips may be programmed to operate at either 531.125 or 1060.25 kbits/s and feature local loopback capability. The chips will also support transmission over fiber-optic or 50-Ω coaxial cable. Packaged in idustry standard M-Quad 80 lead packages, the chips are priced at $55 each in quantities of 1000. Both devices are available immediately. LG

***Hewlett Packard Company, 5301 Stevens Creek Blvd., Santa Clara, CA. 95052-8059; (800) 357-7715, ext. 8364.*** **CIRCLE 672**

## SMT INDUCTOR BLOCKS QUENCH RIPPLE, NOISE

A line of ferrite-core inductors adapted for use in surface-mount assemblies meets even the most stringent requirements for high-current ripple and noise filters. The inductor blocks feature wide bandwidth, low dc resistance and ac losses, and flat frequency and current responses. Standard inductances range from 10 μH at 4 A to 1 mH at 400 mA. Other custom values are available. The blocks are intended as an alternative to toroidal designs and ensure superior power handling. The highly ruggedized package offers easily inspectable, wide surfaces that maximize solder contact. Call for pricing. Production delivery will begin in October. DM



***GFS Magnetics Inc., 140 Crosby Rd., Dover, NH 03820-4371; Jim Radzelovage, (603) 742-4375.*** **CIRCLE 666**

## GASKETS PROVIDE TOUGH EMI SHIELD

A line of plated woven EMI gaskets provides a higher level of shielding than has been available until now. They come in a variety of shapes and sizes to fit many applications, including custom designs. ElectroShield gaskets deliver 130 dB shielding effectiveness at 1 GHz, compared to 100 dB or less for typical high-end solutions. Advanced composite technology is used to completely silver-plate nylon filaments formed around a foam core. Maximum conductivity is assured by the coating technology. A special coating passivates the surface for better corrosion resistance than other silver-plated products. In addition, the gaskets are lightweight and have low closure force and connection set. Available in a wide range of plated nylons, profiles, and core materials, price varies with the many variations of the product. JS

***Instrument Specialties Inc., Delaware Water Gap, PA 18327; (717) 424-8510.*** **CIRCLE 667**

## ENCAPSULATED SENSORS SHRUG OFF CORROSION

A line of metal-encapsulated fluid-level sensors, specifically designed to measure temperature, are ideal for use in applications ranging from chemical processing to petroleum refining. Encased in a noncorroding CrNiMo steel housing, the sensors are oblivious to potentially corrosive materials, such as oil, gasoline, and detergent solutions. The sensors are available in two different temperature ranges, -25°C to +50°C, or +10°C to +90°C. Samples are available from stock and production quantities of the sensors have delivery times of about 12 weeks. The sensors cost about $5.00 each. CA

***Siemens Components Inc., Special Products Division, 186 Wood Ave., South Iselin, NJ, 08830; Ullrich von Seckendorff, (908) 603-5919.*** **CIRCLE 668**

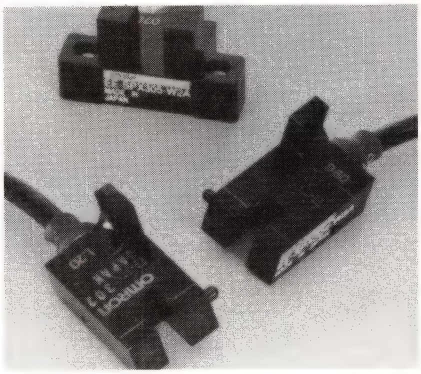
## HIGH-SPEED VCXOs AID NETWORK DESIGNS

A series of high-speed voltage-controlled crystal oscillators (VCXOs) is available for use in the emerging generation of voice-data highways over fiber networks. The VC-6700 Series VCXOs feature ±3% linearity and wide dynamic range of 240 ppm. In designing phase-locked loops, the devices' linearity helps keep gain from varying with frequency, which can adversely impact data integrity. The units offer center-frequency outputs from 40 MHz to 139.264 MHz and 155.520 MHz for use in standard SONET networks in North America and SDH optical networks in Europe and Asia, respectively. Mid-point accuracy is ±15 ppm, and the units are specified to remain within ±20 ppm over the full operating-temperature range of zero to 70°C. Pricing is from $35 to $120 apiece in lots of 10,000. Delivery is in four weeks from receipt of order. DM

***Raltron Electronics Corp., 2315 N.W. 107th Ave., Miami, FL 33172; (305) 593-6033.*** **CIRCLE 669**

## PHOTOSENSORS BLIND TO AMBIENT LIGHT

Pulse modulation is used in the EE-SPX-W2 Series of slotted, amplified, transmissive photomicrosensors to eliminate sensing problems associated with ambient light. Versatile mounting configurations and an attached 2-meter cable allow the devices to address numerous applications without the expense of cabling. The sensors require a 5-to-24-V dc supply and can detect objects as small as 0.5 mm in diameter. Electrical output configurations are light-on or dark-on logic. Each sensor has a red LED that indicates operation. Frequency response is 500 Hz. Pricing starts at $38. Delivery is from stock. DM



***Omron Electronics Inc., One E. Commerce Dr., Schaumburg, IL 60173; (800) 556-6766.*** **CIRCLE 670**

## LOW-POWER OSCILLATOR OFFERS HIGH STABILITY

A high-stability, third-overtone, SC-cut crystal is at the heart of a microcomputer-controlled crystal oscillator from Q-Tech. Microcomputer compensation is employed instead of an oven to achieve stability of $\pm3\times10^{-8}$ ppm. With maximum power consumption of 75 mW, the oscillator is well suited for battery-powered applications where the power-consumption demands of an ovenized oscillator are too great. It's also suited for uses requiring fast warmup and high accuracy. Standard output frequencies are 10 MHz, 4 kHz, and 1 pulse/s. Other frequencies are available optionally on special order. Commercial versions are priced from $559 in lots of 500. DM

***Q-Tech Corp., 10150 W. Jefferson Blvd., Culver City, CA 90232-3502; (310) 836-7900.*** **CIRCLE 671**

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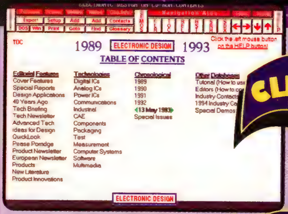

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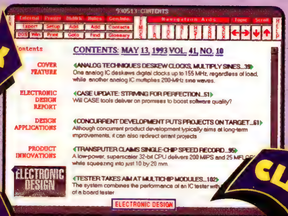

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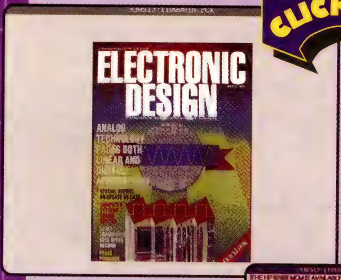

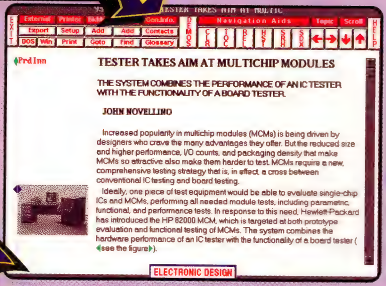

TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is being driven by designers who crave the many advantages they offer. But the reduced size and higher performance, I/O counts, and packaging density that make MCMs so attractive also make them harder to test. MCMs require a new, comprehensive testing strategy that is, in effect, a cross between conventional IC testing and board testing.

Ideally, one piece of test equipment would be able to evaluate single-chip ICs and MCMs, performing all needed module tests, including parametric, functional, and performance tests. In response to this need, Hewlett-Packard has introduced the HP 82000 MCM, which is targeted at both prototype evaluation and functional testing of MCMs. The system combines the hardware performance of an IC tester with the functionality of a board tester (see the figure).

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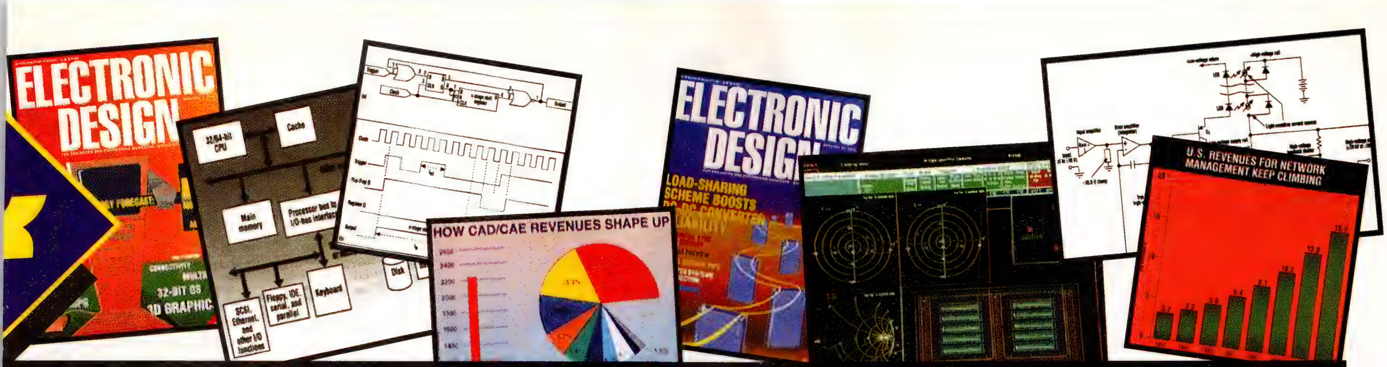
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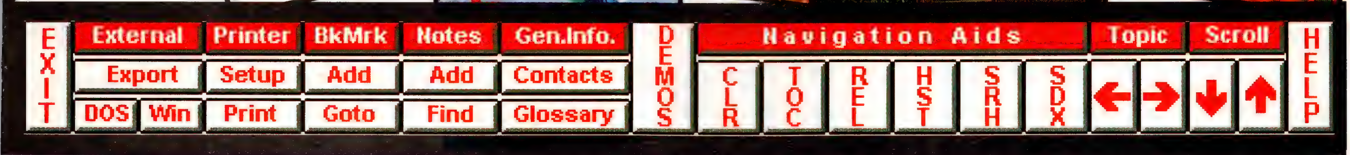

# Learn the backbone of the Electronic Design Magazine CD-ROM interface - the BUTTONBAR.

Powerful, hypertext-based commands let you quickly and efficiently find, re-find, link, make notations, leave bookmarks, export, print, search, get product demos, and even return to your operating system!

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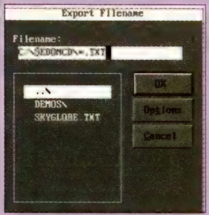

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DOS brings you to the DOS prompt screen and Win takes you into Windows™ without quitting the application. These buttons make it easy for you to return to Electronic Design Magazine, where you left off, without re-launching.

## Printer Commands

**Setup & Print** - This feature allows you to print articles, editorials, glossaries, illustrations, and even photos *(if your printer is capable)* directly from this CD. Great source for reference.

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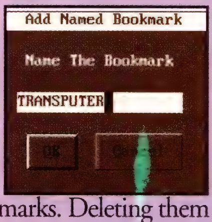

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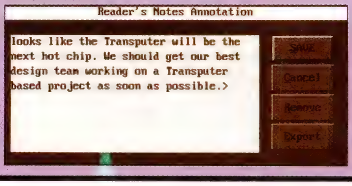

```
looks like the Transputer will be the
next hot chip. We should get our best
design team working on a Transputer
based project as soon as possible.>
```

## Gen. Info - Complete reference

**Contacts** - Company names, addresses, contact names, phone numbers- all of the information you need to follow up.

**Glossary** - Full article glossaries, provided by the Editors of Electronic Design magazine. The CD also comes with **WORD LINK**, which allows you to click on any word within the article and if it's in the glossary, the definition pops up. When you're done, a simple click and it's gone.

## Navigation Aids - Magellan you're not, and you don't need to be!

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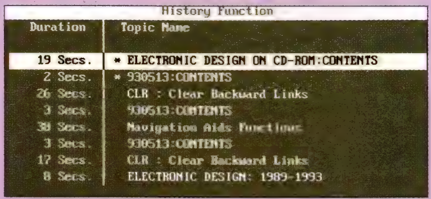
CLR - *Clear Back Links* - Because every article you move to loads into RAM, this function allows you to clear articles you've finished. This frees up RAM for you to continue.

TOC - *Table of Contents* - Takes you directly to the Volume Table of Contents (the whole year) with special links provided to Issue T.O.C.



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  2 Secs.   * 930513:CONTENTS
 26 Secs.     CLR : Clear Backward Links
  3 Secs.     930513:CONTENTS
 38 Secs.     Navigation Aids Functions
  3 Secs.     930513:CONTENTS
 17 Secs.     CLR : Clear Backward Links
  8 Secs.     ELECTRONIC DESIGN: 1989-1993
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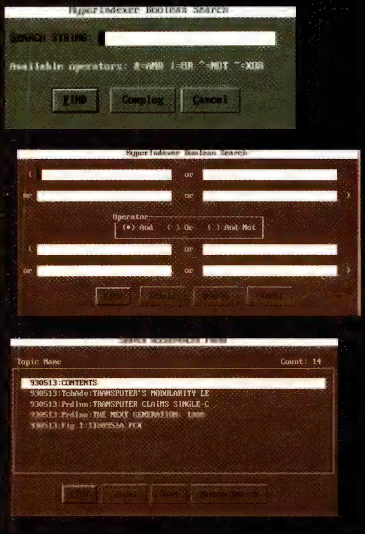
REL - *Show-Related Articles* - Calls up a list of, and lets you move to, related topics.

HST - *Show-Related History* - Shows each topic visited during your current session and how long you were there, and then lets you return to previous topics.

### SEARCH dialog boxes

*Simple search (top), Complex Search (center), and Search occurances found (bottom).*



SEARCH STRING:

Available operators: &=AND |=OR ^=NOT ~=XOR

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930513:PrdInn:TRANSPUTER CLAIMS SINGLE-C
930513:PrdInn:THE NEXT GENERATION: 1000
930513:Fig 1:1100951A PCX
```

SRH - *Search* - Conduct simple, complex or proximity indexed searches.

SDX - *Subject Index* - A hierarchical list of key subject areas compiled by the Editors of Electronic Design. The index also allows direct access to related topics.

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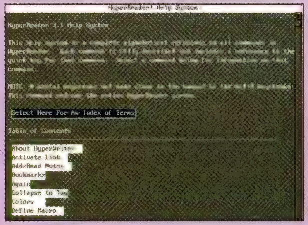

HyperReader 3.1 Help System

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## MINIMUM SYSTEM REQUIREMENTS

- ☞ 80386 PC or better
- ☞ VGA video card adaptor w/640 x 480 pixel resolution 16 colors.
- ☞ 1 meg ram
- ☞ MS-DOS Version 3.1 or later

## BOARD RIGIDIZERS FEATURED IN BROCHURE

Detailed descriptions of various problem-solution situations dealing with board rigidizers and power-distribution issues are contained within a two-page brochure from Circuit Components Inc., Tempe, Ariz. Each case shows how designers used board stiffeners and bus bars to resolve problems related to pc-board warpage, power-distribution problems stemming from space constraints, and solder-joint cracking caused by excess vibration. DM

**CIRCLE 680**

## BROCHURE AUGMENTS OP-AMP DATABOOK

A brochure detailing voltage- and current-feedback op amps and buffers with bandwidths ranging from 45 to 850 MHz provides a quick, comprehensive reference to parts introduced since publication of the 1306-page Linear and Telecom ICs handbook from Harris Semiconductor, Melbourne, Fla. The brochure, called High-Performance Op Amps and Buffers, explains an array of architectural features that broaden the possibilities for device selection. These include multi-amp configurations that provide per-amplifier enable/disable for simple signal multiplexing. Call (800) 442-7747 and ask for Document BR-044NA. DM

**CIRCLE 681**

## 1994 DATA ACQUISITION BOOK

The 1994 long-form data acquisition data book is now available from Harris Semiconductor, Melbourne, Fla. The 1,104-page databook, called Data Acquisition 1994, provides long-form data sheets on hundreds of products for commercial and industrial applications, as well as 39 recently introduced products. Separate sections covering a-d converters include displays, integration, successive approximation, flash, and subranging. Other sections include d-a converters, switches, multiplexers, RS-232 communications interface ICs, display drivers, counters with display drivers/timebase generators, and special-purpose ICs. Data Acquisition 1994 also includes a section that lists application note abstracts. Other sections detail Harris quality and reliability, packaging and ordering information, how to use Harris AnswerFAX, and worldwide sales office contacts. To order this databook, call 1-800-4-HARRIS, ext. 7221. CM **CIRCLE 682**

## CIRCUIT BREAKERS RANGE THROUGH 50 A

A growing line of thermal and magnetic circuit breakers is detailed in the 20-page Catalog 13C322 from Potter & Brumfield Inc., Princeton, Ind. Products offer current ratings from 250 mA through 50 A. Both push-to-reset and switchable types are included. Users may select from pushbutton-, toggle-, and rocker-actuated breakers. A selector guide provides basic information to help readers quickly determine which circuit-breaker series might be best suited for their application. It guides the reader directly to the pages carrying detailed information. DM

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## PCMCIA CONNECTORS ARE BROCHURE'S FOCUS

Complete technical specifications and ordering information on a broad line of sockets and plugs meeting PCMCIA and JEIDA standards are contained within a Sudden Solution guide from Samtec Inc., New Albany, Ind. Standard plugs (PCMP Series) are offered in traditional horizontal through-hole and SMT versions. Vertical-mount designs are also available. The socket (PCMS Series) comes in a straddle-mount design for connecting to both sides of the board. The technical data is supplemented by photos, dimensional drawings, and lists of features. DM

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## FIBER-OPTIC PRODUCTS DETAILED IN CATALOG

A catalog of fiber-optic products from Alpha Wire Corp., Elizabeth, N.J., gives technical standards and specifications for each product to help determine the correct cable for a given application. The catalog also contains a technical glossary, cable-specifications selector guide, conversion chart, and cross reference to further assist in design and specification of fiber optics. DM **CIRCLE 685**

## RF-DEVICE DATABOOK OFFERS VARIETY

Bipolar, LDMOS, MOSFET RF power, and gallium arsenide chip technologies are covered in the 1994 RF Device Databook (DL110/D Rev 5) from Motorola's Semiconductor Products Sector, Phoenix, Ariz. The book presents technical information for several product families. A variety of ceramic and plastic surface-mount packages are covered. Discrete components, hybrid modules, and integrated circuits are detailed. For a free copy of Motorola's 1994 RF Device Databook, call the company at (800) 441-2447, or fax a request to Motorola at (602) 994-6430. DM

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## CONNECTOR PRODUCTS SPAN DENSITY GAMUT

An extensive line of high-density connectors is featured in a 32-page connector-products catalog from JAE Electronics Inc., Irvine, Calif. Products covered include PCMCIA memory-card connectors, surface-mount types, through-hole connectors, wire-to-wire models, I/O connectors, and contact termination tooling. A custom-connector guide allows readers to request special connectors. Photos, mechanical drawings, features, general specifications, materials and finishes, and ordering information are all included in the free connector-products catalog. DM **CIRCLE 687**

## CATALOG DETAILS BATTERIES, ACCESSORIES

A catalog from Power Express, San Jose, Calif., lists long-lasting rechargeable battery packs and battery accessories for notebook and laptop computers, cellular phones, and camcorders. The catalog includes new nickel metal hydride (NiMH) batteries that last 30% longer than standard NiCAD batteries as well as ac adapters, carrying cases, battery maintenance software, and other power accessories. Batteries are available for more than 3000 models, ranging from the newest notebook to the oldest cellular phone. The free catalog includes a battery-management guide that helps consumers increase their battery life. SVT

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# READERS' COMMENTS

## INTERNET: GET WITH IT, VENDORS!

According to your May 16 Editorial (p. 16), you're looking for suggestions on practical ways to use the Internet. It amazes me that electronics vendors are so backward in their use of this priceless resource. How many advertisers in *Electronic Design* even give an e-mail address in their ads? Even vendors of products which have significant software components seem to prefer to make updates available on bulletin boards, instead of by Internet ftp. Bulletin boards! Please! This is 1994, folks, not 1974! Why should I have to make a long-distance phone call to get a software upgrade?

Properly used, an ftp server would be a powerful marketing tool. Instead of calling a company's sales department....making the receptionist understand what I want....getting transferred to somebody who's on another line....finally getting a promise that something will be put in the mail and might reach me in a week—I could browse through all the company's product documentation and sales literature, at negligible cost either to the vendor or to me.

Can you spread the word to vendors? You'd benefit this whole industry tremendously.

**DR. NICK JACOBS**

*Editor's note: This is one of many e-mail letters we received in response to our May 16 Editorial, "Internet." We invite all readers to use this medium to make themselves heard. Again, our Internet address is edesign@class.org.*

## REGARDING THAT 40-YEAR-OLD VTR...

In your article on the video tape recorder article ("40 Years Ago," May 16, p. 8), I think you incorrectly assumed that the word "bit" must have meant *digital* bit. Given the technology of the time, they almost certainly meant "analog bit" (or, more correctly, a spread-spectrum "slice").

To be very loose with the technical details, what these early VTR designers probably attempted to do was convert *high-speed* (wide bandwidth) *serial* analog information into *low-speed* (narrow-bandwidth) *parallel* analog information which fixed tape heads can handle. I would be surprised if the digital equivalent of this technique (combined with image data compression) weren't being used today to transmit full-motion, full-detail digitized video over multiple, low-bandwidth phone lines!

What they probably did was to simply use a 10-tap magnetic delay line driven at a pulse rate of 678 kHz, thus producing an output similar to what we would get using a CD4017 1-of-10 Johnson counter. The delay would have been such that each of the 678-kHz pulses at the taps would have had a phase delay of 36 degrees compared with the tap preceding it.

Each tap was probably then fed to an analog switch and a sample-and-hold (probably implemented as a vacuum-tube switch with a small "hold" capacitor tied to its output). This would have produced a crude spread-spectrum encoder, whereby top-end frequencies (those far above the Nyquist frequency) would be effectively divided by 10 and "spread" across ten 339-kHz channels, creating an *effective* bandwidth of 3.39 MHz. Upon playback, the system probably sync'd the 678-kHz pulse generator to the tape's sync channel, and reversed the process to restore the high-end frequencies.

My guess is that the system was sensitive to tape jitter, which would have almost certainly knocked the 678-kHz pulse generator out of sync temporarily; Also, harmonic distortion (and thus waveshape distortion) must have been terrible.

On the plus side, a tapped delay line cannot "lose count" like a Johnson counter might. Also, interestingly enough, the low-end frequencies (those well below the Nyquist frequency of 339 kHz) would not have been divided at all, but would have simply been duplicated intact on all 10 channels. Since only the top-end frequencies needed to be "reassembled" anyway, slight jitter probably created nothing worse than ragged edge detail on B&W. However, phase jitter would have probably made a big mess of color video!

I'm sure that Bob Pease would agree that there's a LOT to be said for old analog techniques like this, although a PLL and modern DSP techniques would certainly have improved performance considerably.

**CHARLES BARRETT**
**DALLAS SEMICONDUCTOR CORP.**

## COMING: A FLYING CARPET/AIR TAXI

There will soon be a high tech alternative to the automobile that will not get stuck in traffic on I-80. I estimate that about 5% of the population will use this alternative, but very few people will own one. It's a virtual flying carpet that passengers will use to fly from where they are to where they want to be, at any time, at 200-300 mph.

This flying carpet/air taxi will be used on trips of 10-800 miles. The estimated cost per passenger mile is about 20-40 cents for a shared ride, including purchase, maintenance, pilot, interest, advertising, traffic control, and other costs, including fuel at 50 passenger miles per gallon.

The air taxi will require a tremendous amount of electronics, so it's only become possible in the 1990s. Over 1000 MIPS of computing power is needed. All avionics, including radar, GPS, cellular and inter-vehicle communications, will be miniaturized and weigh less than 300 pounds.

No, this is not pie in the sky. Over $35 million has been invested in this air taxi design already. There are deposits for more than 100 vehicles. The design is sound, based on conventional engineering, and has been confirmed by several aerospace companies. It weighs 2400 lbs. and has eight rotary engines with over 1.5 horsepower per pound for a total of 1200 hp. The Moller company group has been producing unmanned air vehicles for over 8 years. Unfortunately, initial operations are likely to be outside the U.S., probably in the Far East where there's more growth, worse traffic problems, and a desire to exploit new concepts.

**HENRY LAHORE**
**SEATTLE, WASH.**

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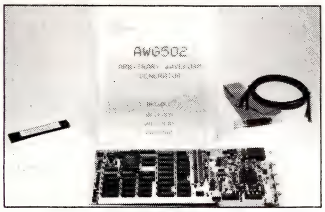

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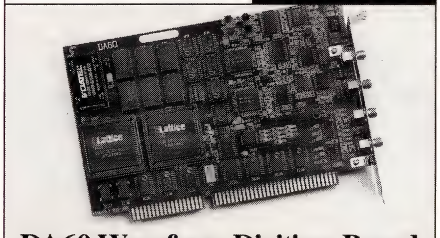

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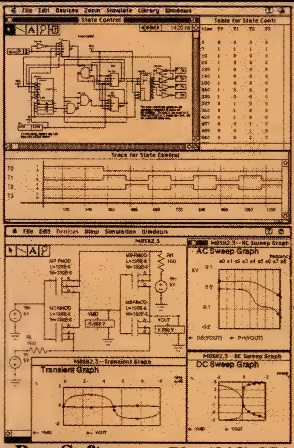

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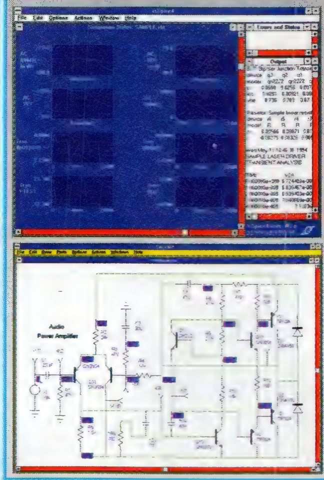

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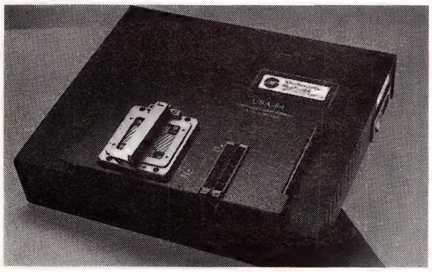

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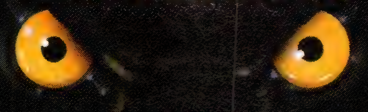

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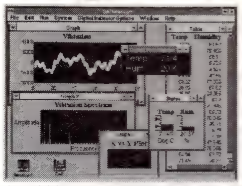

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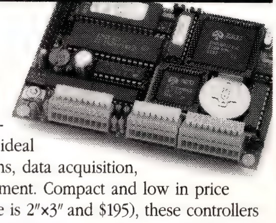

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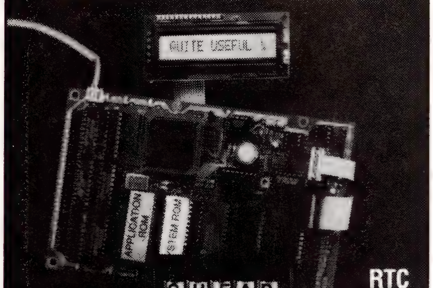

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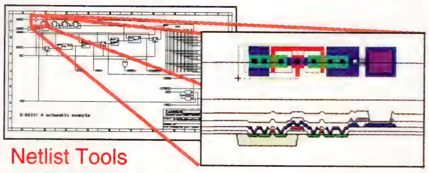

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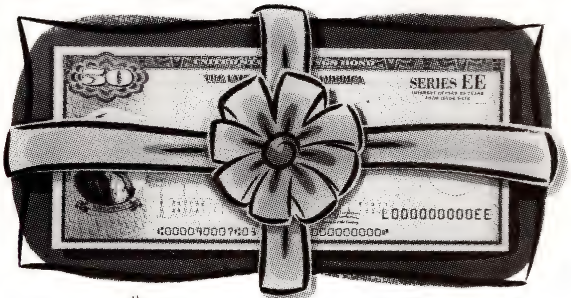

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### JULY

**2nd IEEE Workshop on Real-Time Applications, July 21-22.** Washington D.C. Contact Alexander D. Stoyenko, Real-Time Computing Lab, Computer & Information Science, New Jersey Institute of Technology, University Heights, Newark, NJ 07102; (201) 596-5765; fax (201) 596-5777; E-mail: Alex@vulcan.njit.edu.

**IEEE Power Engineering Society Summer Meeting, July 24-28.** Hilton Hotel, San Francisco, CA. Contact Eva Tiffer, Pacific Gas & Electric Co., Mail Code B23C, P.O. Box 770000, San Francisco, CA 94105; (415) 973-2875; fax (415) 972-6011.

### AUGUST

**MACWORLD Expo/Boston, Aug. 2-5.** Bayside Expo & World Trade Center, Boston, MA. Contact Mitch Hall & Associates at (617) 361-2001.

**3rd IEEE International Symposium on High Performance Distributed Computing, Aug. 3-5.** Westin St. Francis Hotel, San Francisco, CA. Contact Geoffrey C. Fox, NPAC Director, Room 3-228, 111 College Pl., Syracuse, NY 13244-4100; (315) 443-4741; fax (315) 443-1973; E-mail: Gcf@pac.syr.edu.

**4th IEEE Workshop on Computers in Power Electronics, Aug. 7-10.** The Universite du Quebec, Trois-Rivieres, Quebec, Canada. Contact Adam Skorek, Dept. d'Ingenierie, UQTR, C.P. 500, Trois-Rivieres, Quebec G9A 5H7, Canada; (818) 376-5071 ext. 3929; fax (819) 376-5152.

**IEEE International Symposium on Applications of Ferroelectrics, Aug. 7-10.** Conference Center, University Park, PA. Contact Amar Bhalla, 253 MRL, Pennsylvania State University, University Park, PA 16802; (814) 865-9232.

**IEEE International Geoscience & Remote Sensing Symposium (IGARSS '94), Aug. 8-12.** California Institute of Technology, Pasadena, CA. Contact Tammy I. Stein, IEEE/GRSS, 2610 Lakeway Dr., Seabrock, TX 77586; (713) 291-9222; fax (713) 291-9224.

**IEEE Magnetic Recording Conference (IMRC '94), Aug. 16-20.** University of California, La Jolla, CA. Contact Roger F. Hoyt, IBM Almaden Research Center, 650 Harry Rd., K01/803, San Jose, CA 95120-6099; (408) 927-2118; fax (408) 927-3204.

**IEEE International Symposium on Electromagnetic Compatibility, Aug. 22-26.** Palmer House Hotel, Chicago, IL. Contact H.R. Hofmann, 1210 Lawn Meadow Ln., Naperville, IL 60540; (708) 979-3627; fax (708) 979-5755.

**Conference on Lasers & Electro-Optics, Europe & The 5th European Quantum Electronics Convention, Aug. 28-Sept. 2.** RAI Congress Centre, Amsterdam, The Netherlands. Contact Susan Evans, IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3896; fax (908) 562-1571.

### SEPTEMBER

**IEEE International Symposium on Compound Semiconductors, Sept. 18-22.** Del Coronado Hotel, San Diego, CA. Contact James Harbison, Bellcore, 331 Newman Springs Rd., Room 3X-211, Red Bank, NJ 07701; (908) 758-3386; fax (908) 758-4372.

**14th IEEE International Semiconductor Laser Conference, Sept. 19-23.** Hyatt Regency Maui, Maui, HI. Contact Samantha H. Phillips, IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331; (908) 562-3894; fax (908) 562-1571; E-mail: s.phillips@ieee.org.

**ASIC Conference and Exhibit (ASIC '94), Sept. 19-23.** Rochester Riverside Convention Center, Rochester, NY. Contact Paul P.K. Lee, Eastman-Kodak Co., Rochester, NY 14650-2008; (716) 477-2869; fax (716) 477-4947.

**AUTOTESTCON '94, Sept. 20-22.** Disneyland Hotel, Anaheim, CA. Contact Robert Rassa, ManTech International, 150 S. Los Robles Ave., Suite 350, Pasadena, CA 91101; (818) 577-7100; fax (818) 577-7102.

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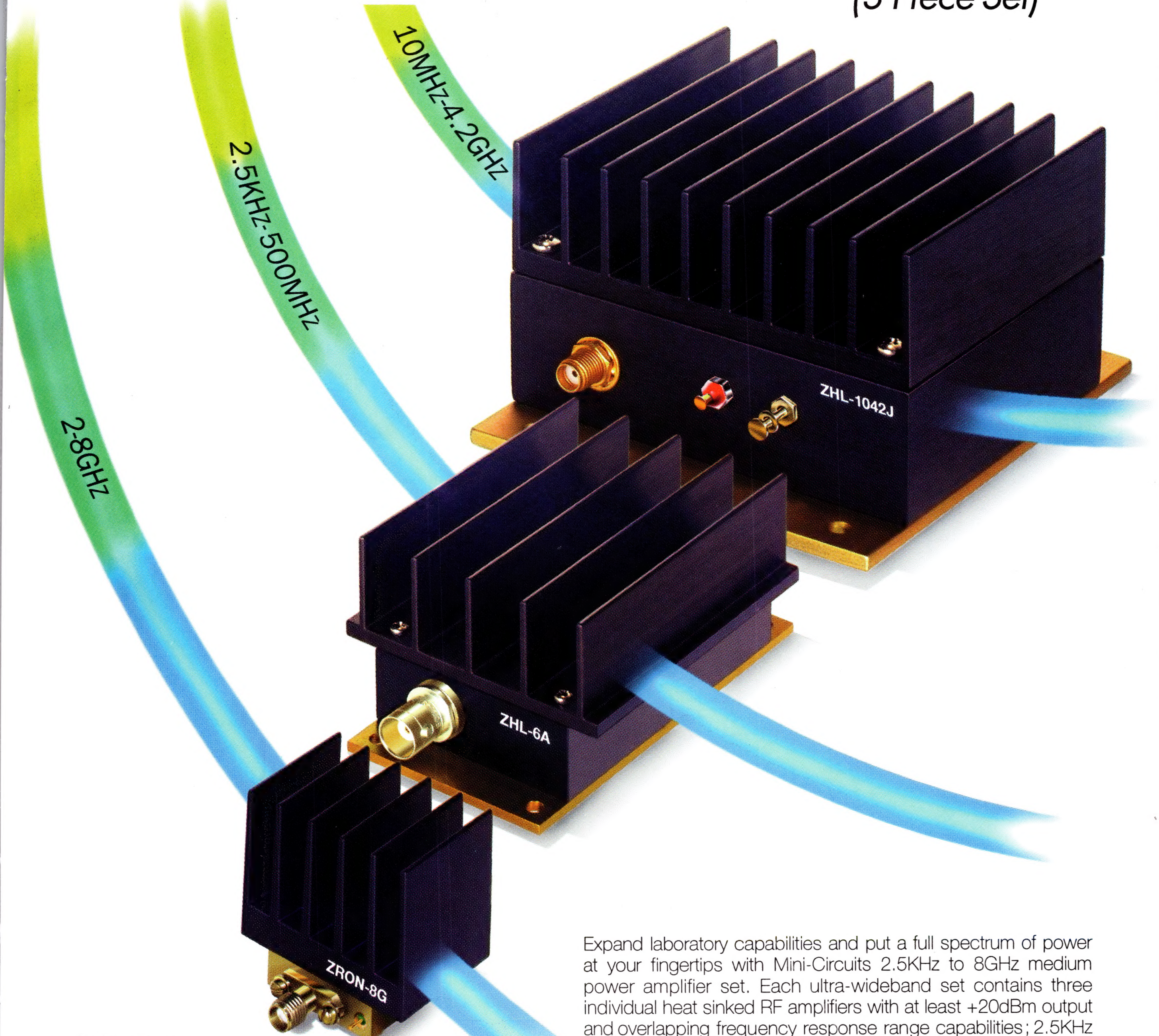

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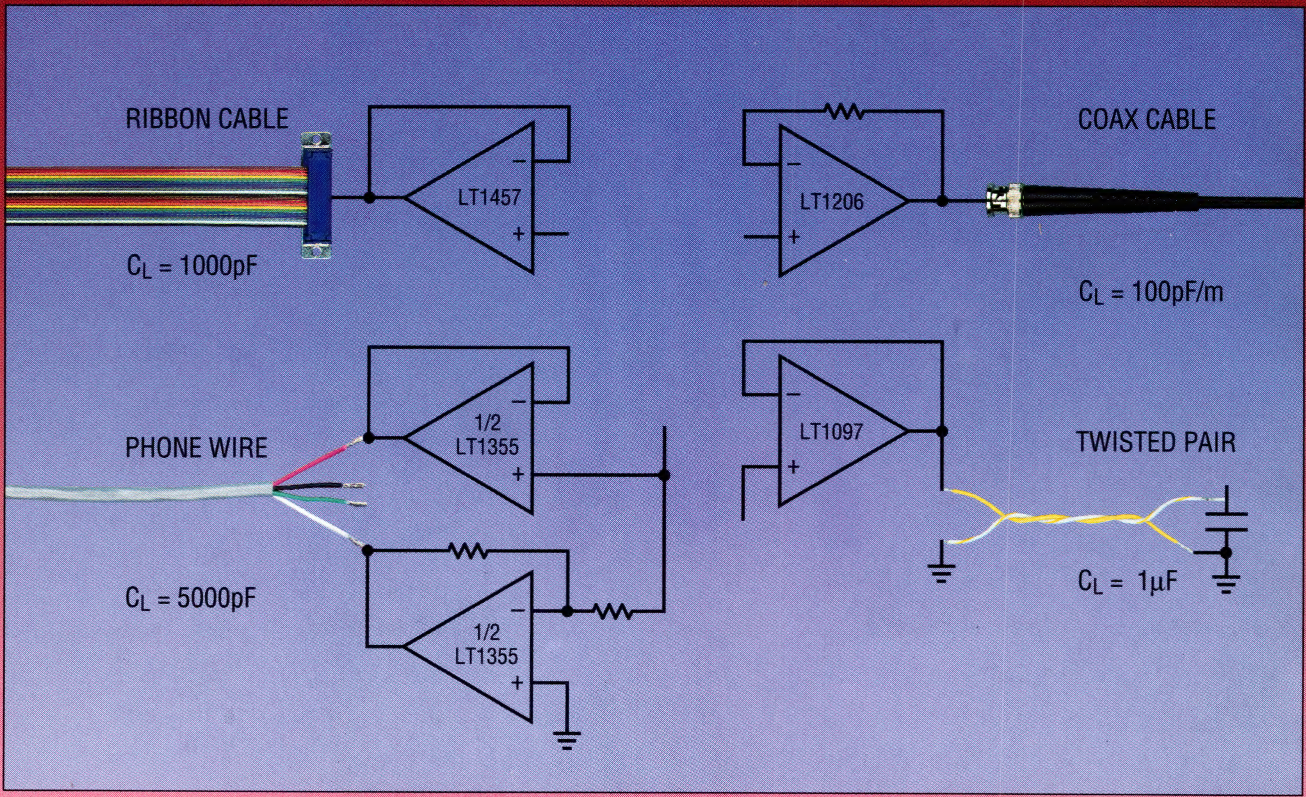

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